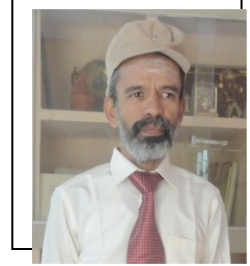


National Institute of Technology, Tiruchirappalli: Performa for CV of Faculty/ Staff Members

Curriculum Vitae



Brief Profile:

Dr. N. Ramasubramanian is a Professor in the Department of Computer Science and Engineering at National Institute of Technology, Tiruchirappalli, India. He did his BE (Electronics and Communication Engineering) and ME in CS from REC TRICHY and Ph.D. from the National Institute of Technology - Tiruchirappalli, Tamil Nadu. He worked as Senior Project Officer in the Department of CSE, Indian Institute of Technology, Madras from 1989-91 and as a Lecturer at ANNA UNIVERSITY MIT CAMPUS Madras during 1991-96. He is working at NIT Trichy from Aug 1996. His research interests include Multi-core architectures, Advanced Digital Design, Processor Architectures for ML and AI, Reconfigurable Computing, and Security Hardware. He is a Member of the Infosys Science Foundations, Bangalore since 2009.

1. Name: Dr. N. Ramasubramanian
2. Designation: Professor
3. Office Address: Department of CSE,
National Institute of Technology,
Tiruchirappalli -620015
4. Telephone (Direct) (Optional):
Telephone: 0431 2503204
5. Email (Primary): nrs@nitt.edu
6. Field(s) of Specialization:
 - Multi-core Computer Architecture
 - Advanced Digital Design
 - Reconfigurable computing
 - Processor Design for ML and AI
 - Security Hardware

National Institute of Technology, Tiruchirappalli: Performa for CV of Faculty/ Staff Members

7. Employment Profile

Job Title	Employer	From	To
Senior Project Officer - VOIS Project	IIT, Madras.	Sept. 1989	Apr. 1991
Lecturer – MIT CAMPUS MADRAS	Anna University	Oct 1991	Aug. 1996
Assistant Professor – CSE	NIT, Tiruchirappalli	Aug. 1996	Dec. 2005
Associate Professor – CSE, (As per VI pay commission)	NIT, Tiruchirappalli	Jan. 2006	Dec 2018
Professor	NIT, Tiruchirappalli	April 2018	Till Date

8. Academic Qualifications (From Highest Degree to High School):

Examination	Board / University	Year	Division/ Grade	Subjects
Ph. D. (CSE)	REC/ NIT, Tiruchirappalli	2012		CSE
M. E. (CSE)	REC/ NIT, Tiruchirappalli	1988-89	First Class with Distinction	CSE
B. E. (ECE)	REC/ NIT, Tiruchirappalli	1984-85	First Class with Distinction	ECE

9. Academic/Administrative Responsibilities within the University

Position	Faculty/Department/Centre/Institution	From	To
Head of CSE Department	Department of CSE	Dec. 2005	Mar. 2009
Additional Chief Warden, Hostel Administrative Committee	NIT, Trichy	Sept. 2015	Feb. 2018
Chairman, PAC	Dept. of CSE (UG/ PG)	Jul. 2006	Ongoing
Ph.D. Admissions	Dept. of CSE	Oct. 2006	Ongoing

10. Academic/Administrative Responsibilities outside the University

Position	Institution	From	To
Member Board of Studies	SASTRA	2008	2012
Member Board of Studies	Anna University, Chennai	2009	2012
Ph. D. Examiner	Anna University, Chennai	2012	Till Date

National Institute of Technology, Tiruchirappalli: Performa for CV of Faculty/ Staff Members

11. Awards, Associateships etc.

Year of Award	Name of the Award	Awarding Organization
2015	Distinguished Alumna Award From the HONBLE PRESIDENT OF INDIA	NIT TRICHY
2017 and 2018	For Maximum number of Publications during academic year	NIT TRICHY during Institute Day
2018	Intel “Appreciation award” 2018	Intel India Bangalore

12. Fellowships: NIL

Year of Award	Name of the Fellowship	Awarding Organization	From (Month/Year)	To (Month/Year)

13. Details of Academic Work

I. Curriculum Development

- Orientation towards Computer Engineering/ Computer System Design
- Initiative for enriching the curriculum towards Computer Engineering/ Computer System Design
Outcome: New Courses on Parallel Computer Architecture, Computer System Design Lab and Advanced Digital Design
- Reconfigurable Intelligent System Engineering (**RISE**) Lab (Under TEQIP)- 2007
 - Industry Partners: ARM, Xilinx
 - Academic Partner: IIT, Madras
 - M. Tech. Computer Systems Design Lab course.
Outcome: Ph. D. – 04, M. Tech. Projects – 22, B. Tech. Projects – 14
- Intel Multicore Technology Lab (Intel Sponsored) – 2009
 - M. Tech. Parallel Computer Architecture Assignments.
 - Areas: Multi-core Architectures, Reconfigurable Embedded Data Cache, Cache Coherence, FPGA based Accelerator
Outcome: Ph. D. – 06 ongoing, , B. Tech. Projects – 14

National Institute of Technology, Tiruchirappalli:

Performa for CV of Faculty/ Staff Members

II. Courses taught at Postgraduate and Undergraduate levels

- Core Courses

- Computer Organization
- Computer Architecture
- Digital System Design
- Parallel Computer Architecture
- Computer System Design Lab
- Elements of Computing

- Elective Courses

- Advanced Digital Design
- Principles of Processor Design

III. Projects guided

- M. Tech. Projects – 48
- B. Tech. Projects – 40

IV. Other contribution(s)

MNC Model- Intel/ ARM/ Xilinx - Internship and M. Tech. Projects

Outcome-

- *Donation:* Lab Kits/ ARM Cortex M3 Series Kits/ Intel Galileo Boards

Project Titles:

- “BIOS Design for Thunderbolt in Next Generation INTEL Platform”, at Intel India, Bangalore
- “Implementing DIGRF Driver Host Test with Multiple Execution Context”, at Intel India, Bangalore

14. Details of Major R&D Projects

Title of Project	Funding Agency	Duration		Status
		From	To	Ongoing/ Completed
Energy Efficient Implementation of Multi-Modular Exponential Techniques for	DST, Reference Number: T 895 Rs 30 lahks NIT TRICHY & IIIT RAIPUR	2019	2021	Ongoing

**National Institute of Technology, Tiruchirappalli:
Performa for CV of Faculty/ Staff Members**

Public-key Cryptosystems				
--------------------------	--	--	--	--

15. Number of PhDs guided

Name of the PhD Scholar	Title of PhD Thesis	Role(Supervisor/ Co-Supervisor)	Year of Award
<u>Satyanarayana Vollala</u>	Novel Energy Efficient Modular Exponential Techniques for Public-Key Cryptography	Supervisor	2017
Manjith B. C	Enhancing Performance of FPGA based AES implementations for improved security.	Supervisor	2018
B. Shameedha Begum	Studies on Performance Evaluation of Reconfigurable Embedded Data Cache.	Supervisor	2019

16. Participation in Workshops/ Symposia/ Conferences/ Colloquia /Seminars/ Schools etc. (mentioning the role) :NIL

Date (s)	Title of Activity	Level of Event (International/ National/ Local)	Role (Participant/ Speaker/ Chairperson, Paper presenter, Any other)	Event Organized by	Venue

17. Workshops/ Symposia/ Conferences/ Colloquia/Seminars Organized (as Chairman/ Organizing Secretary/ Convenor / Co-Convenor)

Title of Activity	Level of Event (International/ National/ Local)	Date (s)	Role	Venue
“FDP on Xilinx SoC FPGA Based Design” in collaboration with	National FDP	30 th July to 3 rd Aug	Convener	CSE Digital Systems Lab, NITT

National Institute of Technology, Tiruchirappalli: Performa for CV of Faculty/ Staff Members

Ministry of Electronics & Information Technology (MeitY), Government of India, and the Electronics & ICT Academy IIT Guwahati, Assam		2018		
Two days Workshop on Advanced Embedded System Design on Zynq using Vivado Targeting Zed Board	National Workshop	28th and 29th August 2015	Convener	CSE Digital Systems Lab

18. Invited Talks delivered

Topic	Date	Inviting Organization
Domain Specific Architecture	National College, Trichy September-2018.	International Conference on Blooming Trends in Tech Challenges and Opportunities (BTTCAO), Tamil Nadu, India.

19. Membership of Learned Societies

Type of Membership (Ordinary Member/ Honorary Member / Life Member)	Organization	Membership No. with date
Member	ACM	
Member	IEEE	

20. Academic Foreign Visits NIL

Country	Duration of Visit	Programme

**National Institute of Technology, Tiruchirappalli:
Performa for CV of Faculty/ Staff Members**

21. Publications

(A) Refereed Research Journals:

Author(s)	Title of Paper	Journal	Volume (No.)	Page numbers	Year	Impact Factor of the Journal (Optional)
J. Kokila, N. Ramasubramanian, and Ravindra Thamma	“Dynamic estimation of temporary failure in SoC FPGAs for Heterogeneous Applications”	The Journal of Universal Computer Science, J.UCS Consortium, Austria	24.12	1776-1799.	2019	1.08
Shathanaa R., and Ramasubramanian N.	A Memetic Algorithm based Design Space Exploration for Datapath Resource Allocation during High Level Synthesis.	Journal of Circuits, Systems, and Computers – WORLD SCIENTIFIC			2019	0.595
Shathanaa R., and Ramasubramanian N.	Group influence based improved firefly algorithm for Design Space Exploration of Datapath resource allocation	Applied Intelligence, SPRINGER			2019	1.983
Manjith B.C, Ramasubramanian N.	Securing AES Accelerator from Key-Leaking Trojans on FPGA	International Journal of Information Technology and Web Engineering (IJITWE) - IGI Global			2018	
B. Shameedha begum,	Design of an Intelligent data	International journal of			2018	

**National Institute of Technology, Tiruchirappalli:
Performa for CV of Faculty/ Staff Members**

Ramasubramanian N.	Cache with replacement policy	Embedded and real Time Communication Systems IGI Global				
Anjali A V, N. Ramasubramanian	Indian Language Text Summarization Using Recurrent Neural Networks	International Journal of Computer Sciences and Engineering,	Vol.06, Special Issue.11, pp.162-164, 2018.	112 - 122	2017	UGC Approved IF= 3.022
Anjali T P, N Ramasubramanian	Traffic Sign Recognition Using Optimized Convolutional Neural Network	International Journal of Computer Sciences and Engineering,	Vol.06, Special Issue.11, pp.103-106, 2018.	3105 – 3115	2016	UGC Approved IF= 3.022
Tamizharasan, P. S., and N. Ramasubramanian.	Analysis of Large Deviations Behaviour of Multi-GPU Memory Access in Deep Learning	The Journal of Supercomputing (Springer)	74.5	2199-2212.	2018	1.5
Chellam, Manjith Baby, and Ramasubramanian Natarajan.	"AES Hardware Accelerator on FPGA with Improved Throughput and Resource Efficiency	Arabian Journal of Science and Engineering (Springer)		1 - 18	2017	1.09
Vollala, Satyanarayana, and Natarajan Ramasubramanian	Energy efficient modular exponentiation for public-key cryptography based on bit forwarding techniques	Information Processing Letters (Elsevier)				
Shameedha Begum, T Vidya, Amit D. Joshi and N Ramasubramanian;	A Reconfigurable Cache Design for Embedded Dynamic Data cache	IJCTA	9	8509-8517	2016	0.605

**National Institute of Technology, Tiruchirappalli:
Performa for CV of Faculty/ Staff Members**

Vollala, S., Varadhan, V. V., Geetha, K., & Ramasubramanian, N.	Design of RSA processor for concurrent cryptographic transformations.	Microelectronics Journal (Elsevier)	63	112-122	2017	0.8
Satyanarayana Vollala, K. Geetha and N. Ramasubramanian	Modular Cryptography Exponential Algorithms compatible to Hardware Implementation of Public-Key	Security and Communications Networks (Wiley)	9	3105- 3115	2016	0.81
Singh, A. K., Geetha, K., Vollala, S., & Ramasubramanian, N.	Efficient utilization of shared caches in multicore architectures.	Arabian Journal of Science and Engineering (Springer)	41(12)	5169- 5179	2016	1.09
N.Ramasubramanian, Srinivas V.V and N.A. Gounden	Performance of Cache memory subsystems for multicore architectures	International Journal of Computer Science, Engineering and Applications	1	29-36	2013	
N.Ramasubramanian, Srinivas V.V and Chaitanya V	Studies on performance aspects of scheduling algorithms on multicore platforms	International Journal of Advanced Research in Computer Science and Software Engineering	2	41-44	2013	
N. Ramasubramanian, Hathiram Banoth and P. S. Tamizharshan	Evaluation of Cache Memory Parameters with Different Instruction Set Architectures	International Journal of Computational Engineering & Management	16	64-68	2013	
N. Ramasubramanian, Srinivas V. V. and Praveen Kumar Yadav	Performance Evaluation of Stream Log Collection Using HADOOP Distributed File System	International Journal of Advanced Research in Computer Science and Software Engineering	3		1995	
N.	Improving	International	16	29-36	2013	

**National Institute of Technology, Tiruchirappalli:
Performa for CV of Faculty/ Staff Members**

Ramasubramanian, Ashutosh, Akhilesh Kumar Verma, Manvendra Singh and Praveen Kumar Yadav	Performance of Real Time Scheduling Policies for Multicore Architecture	Journal of Computational Engineering & Management				
N.Ramasubramanian	Modelling Semantic Interdependent Structures using modified Extended Back propagation Neural Networks	International Journal of Management and Systems	2	41-44	2013	

(B) Conferences/Workshops/Symposia Proceedings

Author(s)	Title of Abstract/ Paper	Title of the Proceedings	Page numbers	Conference Theme	Venue	Year
Tamizharasan P S and Ramasubramanian N	Enhancing GPU performance using thread geometry analysis for irregular workloads	4 th international conference on computing in engineering & Technology		computing in engineering & Technology		2019
R.Janbandhu, Ramasubramanian N and Shameedha Begum	Credit card fraud detection	4 th international conference on computing in engineering & Technology		computing in engineering & Technology		2019
Abhijith M, Bhukya Krishna Priya and Ramasubramanian N	Malware Detection in Android using Machine Learning on chip	4 th international conference on computing in engineering & Technology		computing in engineering & Technology		2019
Bhukya Krishna Priya and Ramasubramanian N	SET-CMP: Improving the Lifetime of NVM Cache	4 th international conference on computing in engineering & Technology		computing in engineering & Technology		2019
Bhagya Presannan,N	Disease Risk Prediction	4 th international conference on		computing in engineering &		2019

**National Institute of Technology, Tiruchirappalli:
Performa for CV of Faculty/ Staff Members**

Ramasubramanian and A SanthanaVijayan	from Clinical Texts	computing in engineering & Technology		Technology		
Vollala, Satyanarayana; Ramasubramanian, N; Begum, B Shameedha; Joshi, Amit D;	Dual-Core Implementation of Right-to-Left Modular Exponentiation	Recent Findings in Intelligent Computing Techniques	43-53	Intelligent Computing Techniques		2019
Krishna Priya, Sampath Kumar, N. Ramasubramanian, B. Shameedha Begum;	Enhancing the Lifetime of STT-RAM with MRU Replacement Algorithm	International Conference on Recent Advances in Information Technology(RAIT)		Recent Advances in Information Technology		2018
R. Shathanaa and N. Ramasubramanian	Improving Power & Latency Metrics for Hardware Trojan Detection during High Level Synthesis	International Conferenece on Computing, Communication and Networking Technologies		Computing, Communication and Networking Technologies		2018
Anjali AV , N. Ramasubramanian and A. Santhanavijayan	Text Summarization of Indian languages Using Recurrent Neural Networks	International Conference on Blooming trends in Tech Challenges and Opportunities(BTT CAO)		Blooming trends in Tech Challenges and Opportunities		2018
Anjali TP and N. Ramasubramanian	Traffic Sign Recognition using Optimized Convolutional Neural Network	International Conference on Blooming Trends in Tech Challenges and Opportunities (BTTCAO)		Blooming trends in Tech Challenges and Opportunities		2018
Rajkumar, Shreya, Malavika Srikanth, and N. Ramasubramani	Health monitoring system using Raspberry PI	International Conference on Big Data, IoT and Data Science (BID	116-119	Big Data, IoT and Data Science		2017

**National Institute of Technology, Tiruchirappalli:
Performa for CV of Faculty/ Staff Members**

an.					
Kokila, J., Chellam, M. B., Das, A. M., & Ramasubramani an, N.	Light Weight Two-Factor Authentication Using Hybrid PUF and FSM for SOC FPGA.	International Conference on Next Generation Computing Technologies	381- 395	Next Generation Computing Technologies	2017
Manjith B. C. Kokila, J., Ramasubramani an, N.	Adaptive Dynamic Partial Reconfigurabl e Security System	International Conference on Next Generation Computing Technologies	430- 439	Next Generation Computing Technologies	2017
Kumar, V. Anand Prem, and N. Ramasubramani an	Pre-processing Algorithm for Rule Set Optimization Throughout Packet Classification in Network Systems	Computing and Network Sustainability.	323- 331	Computing and Network Sustainability	2017
R. Shathanaa and N. Ramasubramani an	Design Space Exploration for Architectural Synthesis - A Survey	International Conference on Advanced Computing, Networking, and Informatics		Advanced Computing, Networking, and Informatics	2017
Vollala, Satyanarayana; Begum, B Shameedha; Ramasubramani an, N;	Evaluation of password encrypted key exchange authentication techniques: design approach perspective: evaluation of PAKE protocol	Proceedings of the 1st International Conference on Internet of Things and Machine Learning	16	Internet of Things and Machine Learning	2017
Joshi, Amit D; Indrajeet, S; Ramasubramani an, N; Begum, B Shameedha;	Analysis of multi-core cache coherence protocols from energy and	Recent Innovations in Signal processing and Embedded Systems (RISE), 2017 International	381- 388	Recent Innovations in Signal processing and Embedded Systems	2017

**National Institute of Technology, Tiruchirappalli:
Performa for CV of Faculty/ Staff Members**

	performance perspective	Conference on		(RISE)		
Joshi, Amit D; Vollala, Satyanarayana; Begum, B Shameedha; Ramasubramanian, N;	Performance Analysis of Cache Coherence Protocols for Multi-core Architectures: A System Attribute Perspective	Proceedings of the International Conference on Advances in Information Communication Technology & Computing	22	Advances in Information Communication Technology & Computing		2016
Vollala, Satyanarayana; Begum, B Shameedha; Joshi, Amit D; Ramasubramanian, N;	High-radix Modular Exponentiation for hardware implementation of Public-Key Cryptography	Computing, Analytics and Security Trends (CAST), International Conference on	346-350	Computing, Analytics and Security Trends (CAST),		2016
Begum, B Shameedha; Krishnakumar, Arun; Joshi, Amit D; Ramasubramanian, N;	Design of a Reconfigurable Embedded Data Cache	Computing, Analytics and Security Trends (CAST), International Conference on	318-322	Computing, Analytics and Security Trends (CAST),		2016
Kokila, J., N. Ramasubramanian, and S. Indrajeet	A survey of hardware and software co-design issues for system on chip design	Advanced Computing and Communication Technologies.	41-49	Computing and Communication Technologies		2016
Tamizharasan. P ; Karthikeyan. M, Ramasubramanian. N, Joshi. A	Performance Enhancement of Phoneme Recognition using GPUs	International Conference on Communication and Signal Processing (ICCASP 2016)	531-537	Communication and Signal Processing		2016
Yadav.P , Ramasubramanian.N, Joshi. A, Tamizharasan.P	Saliency Aware Resource Saving in Hand-Held Devices	International Conference on Communication and Signal Processing	499-505	Communication and Signal Processing		2016
Raghunathan, M. J., Arjun, V.	A novel scheduling	International Conference	1 to 6	Microelectronics, Computing		2016

**National Institute of Technology, Tiruchirappalli:
Performa for CV of Faculty/ Staff Members**

B., Kaushik, K. S., & Ramasubramanian, N.	algorithm for phase change memory based main memory system with multiple ranks.	on Microelectronics , Computing and Communications (MicroCom), 2016,		and Communicatio ns		
Anand Prem kumar and N. Ramasubramanian	Rule Set Optimization for Packet Pre-processing using Hash based Algorithm	International Conference on Microelectronics Computing and Communication Organized by the Department of Electronics & Communication Engineerin		Microelectroni cs, Computing and Communicatio ns		2016
Begum, B Shameedha; Ramasubramanian, N;	A comparative study of cache performance for embedded applications	Computing and Network Communications (CoCoNet), 2015 International Conference on	872-876	Computing and Network Communicatio ns		2015
Vollala, Satyanarayana; Begum, B Shameedha; Ramasubramanian, N;	Hardware design for multiplicative modular inverse based on table look up technique	Computing and Network Communications (CoCoNet), 2015 International Conference on	520-523	Computing and Network Communicatio ns		2015
Praveen Kumar Yadav, and N. Ramasubramanian	Efficient Resource Utilization in Mobile Devices Using Bayesian Framework Based Saliency Mapping	DRDO Bilingual International Conference, Information Technology : Yesterday, Today, and Tomorrow		Information Technology		2015
Anand Prem Kumar, Vidya Thiyagarajan and N. Ramasubramanian	A Survey of Packet Classification Tools and Techniques	International Conference on Computing, Communication, Control And Automation	103-107	Computing, Communicatio n, Control And Automation		2015
Sangeetha, R. and N.	A survey of hardware	International Conference on	1 to 5	Signal Processing,		2015

**National Institute of Technology, Tiruchirappalli:
Performa for CV of Faculty/ Staff Members**

Ramasubramanian	signature implementations in multi-core systems	Signal Processing, Communication and Networking		Communication and Networking		
Vidya, T. and N. Ramasubramanian	Design of an interconnect topology for multi-cores and scale-out workloads	International Conference on Signal Processing, Communication and Networking	1 to 5			2015
Joshi, Amit D. and N. Ramasubramanian	Comparison of significant issues in multicore cache coherence	International Conference on Computing and Internet of Things	108-112	Conference on Computing and Internet of Things		2015
Vollala, S., Varadhan, V. V., Geetha, K., & Ramasubramanian	Efficient modular multiplication algorithms for public key cryptography	International conference of Advance Computing Conference (IACC), 2014	74- 78	Advance Computing		2014
Yadav, P. K., & Ramasubramanian, N	Power consumption of Android device using different video codecs: An analysis	International conference of Advance Computing Conference (IACC), 2015	1019-1023	Advance Computing		2014
Satyanarayana Vollala, Praveen Kumar Yadav, K.Geetha, N.Ramasubramanian	A Comparative Study on Enhancements Made for RSA Implementation from Hardware Perspective	International Conference on Advances in Computer Science,		Advances in Computer Science		2014
Tamizharasan, P. S., Yadav, P. K., Ramasubramanian, N., & Geetha, K	Performance enhancing factors for manycore architectures: State-of-the-art	In Networks & Soft Computing (ICNSC), 2014 First International Conference	278-283	In Networks & Soft Computing		2014
B. C. Manjith , Praveen Kumar	A Survey of Hardware –	International Conference on		Computer Communicatio		2014

**National Institute of Technology, Tiruchirappalli:
Performa for CV of Faculty/ Staff Members**

Yadav, R. Sangeetha and N. Ramasubramanian	Software Security Architectures to Cloud Server	Computer Communication Networks (ICCN 2014)		n Networks		
N. Ramasubramanian, Praveen Kumar Yadav and K. Geetha	Different Ways of Exploiting User Satisfaction for Quantifying Performance of Embedded System Application	International Conference on CNC&CSEE	447-452	CNC&CSEE		2013
Satyanarayana Vollala, Praveen Kumar Yadav, K. Geetha, N. Ramasubramanian,	A Comparative Study on Enhancements Made for RSA Implementation from Hardware Perspective	International Joint Conference on Advances in Engineering and Technology	169-174	Advances in Engineering and Technology		2013
N. Ramasubramanian and Varadhan V.V.	Estimation of optimum parameters for obtaining enhanced QoS in a virtualized server consolidated cloud environment	International Conference on CNC&CSEE	466-471	CNC&CSEE		2013
Srinivas V.V and N. Ramasubramanian	Understanding the performance of multi-core platforms	International Conference on Computer Networks and Information Technology	22-26	Computer Networks and Information Technology		2011
N. Ramasubramanian, Srinivas V.V and P. Pavan Kumar	Understanding the impact of cache performance on multi-core architectures	International Conference on Information Technology and Mobile Communications	403-406	Information Technology and Mobile Communications		2011

**National Institute of Technology, Tiruchirappalli:
Performa for CV of Faculty/ Staff Members**

Karthik K.S, Shyam.S, Ramasubramani an.N, Shoaib.M, Noor.M and Kamakoti.V	A SEU Tolerant Distributed CLB RAM for In-Circuit Reconfiguratio n	International conference on VLSI Design and Test Symposium	228- 238	VLSI Design and Test Symposium	2009
N.Ramasubram anian, P.Krishnan and V.Kamakoti	Studies on the performance on two new bus arbitration schemes for multi-core processors	International conference on Advanced Computing	1192- 1196	Advance Computing	2008

(C) Books & Monographs:

Author(s)	Title of Book/Monograph	Name of Publishers	Year of Publication	ISSN/IS BN Number
N. Ramasubramanian, Manjith B. C	Book chapter in Authentication Technologies for Cloud Technology, IoT, and Big Data, “Cryptography Engines for Cloud Based on FPGA”	IET, UK	2019	978-1- 78561- 556-6
P.S. Tamizhrasan, M. Karthikeyan, Amit D. Joshi and N. Ramasubramanian	Book Chapter in Advances in Intelligent Systems and Research, “Performance Enhancement of Phoneme Recognition using GPUs”	Atlantis Press	2016	
Praveen Yadav P.S. Tamizharasan, Amit D. Joshi and N. Ramasubramanian	Book Chapter in Advances in Intelligent Systems and Research, “Saliency Aware Resource Saving in Hand-Held Devices”	Atlantis Press	2016	
N. Ramasubramanian and T. Vidya	Book Chapter in CMOS Digital VLSI Design with Verilog, “NoC Design for interconnecting Multi- cores”	Springer	2015	