Design and Implementation of MB-OFDM UWB Transceiver Modules using Asynchronous Pipelining - NIT, Trichy

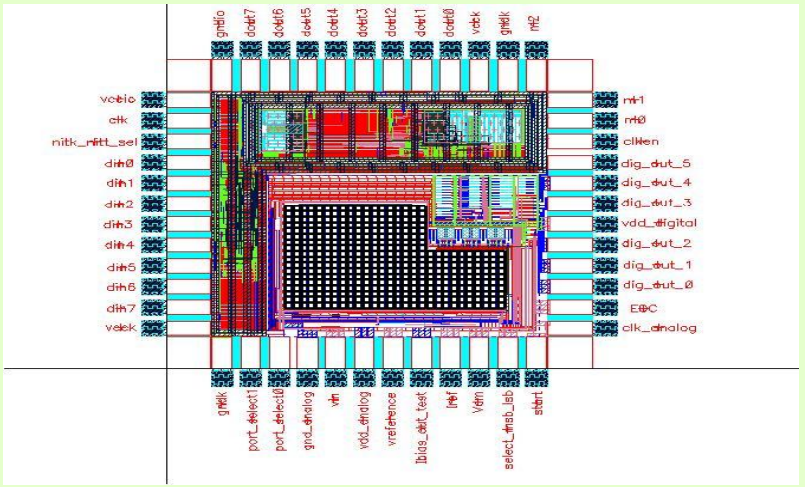
Total Outlay: Rs. 33.50 lakhs **Duration:** 24months (Feb08 – Mar10) **Extension:** 12 months

Achievement/Progress:

- Design and FPGA implementation of MB-OFDM UWB wireless system digital backend modules, ADC/DAC boards and RF frontend boards using synchronous pipelining are completed.
- Design and FPGA implementation of MB-OFDM UWB wireless system digital backend modules using Asynchronous pipelining are completed.
- Integration of digital backend modules with RF frontend modules with wired/ wireless communication is completed.
- ASIC implementation of Digital backend modules using synchronous pipelining is completed.
- To bring improvement, a burst mode operation of UWB system has been carried out using INTASYCON (INTelligent ASYnchronous CONtroller). This is giving very good improvement on Low Power Consumption.

Other outcomes are

- Chip designed using INTASYCON technique is fabricated through IndiaChip programme.
- Initiated collaborative work with SAMEER-CEM, Chennai and Carried out RF front end fabrication and integration
- Published 5 international Journal Papers and 11 International Conference Papers.
- Two are awarded Ph.D degree
- Mr. Sanjay M. Talekar who worked as Scientist in this project has got a job at SAMEER-CEM, Chennai.



Pin Configuration of the fabricated IC