## Annexure-I



Department of Electronics and Information Technology (DeitY)  $\,$ 

Ministry of Communications & Information Technology (Government of India)

Electronics Niketan, 6, CGO Complex,

Lodhi Road, New Delhi: 110003

## Design and Implementation of Low power Analog Frontend modules for Wireless sensor Networks

## 1. Project Outlay

Head	Year			Total
	First	Second	Third	1 Otal
Capital Equipment	5.50	0	0	5.50
Consumable Stores FE Component	0.30	5.40	5.40	11.10
		(USD	(USD	(USD
		10,000)	10,000)	20,000)
Manpower	6.36	6.36	5.28	18.00
Travel & Training	0.30	0.40	0.40	1.10
Contingencies	0.50	0.50	0.50	1.50
Overheads	0.60	0.60	0.60	1.80
Total (FE Component)	13.56	13.26	12.18	39.00
		(USD	(USD	(USD
		10,000)	10,000)	20,000)

2. (a) Contribution of Project Implementing/

& other Organisation in Total Budget Outlay

(Electricity, Internet, lab space, furniture etc): Rs. 0

(b) DeitY Contribution: Rs. 39.0 Lakhs

3. Scheme under which the project has been taken: R & D Funding Scheme

- 4. Date of starting the project: 23.11.2011
- 5. Scheduled date of completion of the project: 22.11.2014
- 6. Implementing Agency: Department of ECE

National Institute of Technology

Tiruchirappalli – 620 015

- 7. Contact details of Chief Coordinator (Implementing Agency) for further information or feedback with website address:
- (i) Chief Investigator:

Name: Dr. B. Venkataramani

Designation: Professor & Dean (R&C)

Department: Department of ECE

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## (ii) Co-Investigator:

Name: Mr. M. Bhaskar

Designation : Associate Professor

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