M. Tech.

IN

VLSI SYSTEM ENGINEERING

CURRICULUM

(For students admitted in 2016-17)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY

TIRUCHIRAPPALLI – 620 015

TAMIL NADU, INDIA

CURRICULUM

The total minimum credits for completing the M.Tech. programme in VLSI System is 66 .

SEMESTER I

Sl. No.	Course Code	Course of	Credits
1.	MA617	Graph Theory and Discrete Optimization	3
2.	EC651	Analog IC Design	3
3.	EC653	Basics of VLSI	3
4.		Elective I	3
5.		Elective II	3
6.		Elective III	3
7.	EC655	HDL Programming Laboratory	2
		Total	**20**

SEMESTER II

Sl. No.	Course Code	Course Title	Credits
1.	EC652	VLSI System Testing	3
2.	EC654	Electronic Design Automation Tools	3
3.	EC656	Design of ASICs	3
4.		Elective IV	3
5.		Elective V	3
6.		Elective VI	3
7.	EC658	Analog IC Design Laboratory	2
8.	EC660	ASIC – CAD Laboratory	2
		Total	**22**

SEMESTER III

Course Code	Course Title	Credits
EC697	PROJECT WORK - PHASE I	12
Total		**12**

SEMESTER IV

Course Code	Course Title	Credits
EC698	PROJECT WORK - PHASE II	12
Total		**12**

LIST OF ELECTIVES

Sl. No.	Course Code	Course Title	Credits
1.	EC661	Digital System Design	3
2.	EC662	Modeling and Synthesis with Verilog HDL	3
3.	EC663	Optimization of Digital Signal Processing structures for VLSI	3
4.	EC664	Cognitive Radio	3
5.	EC665	VLSI Process Technology	3
6.	EC666	Analysis and Design of Digital Systems using VHDL	3
7.	EC667	Advanced Computer Architecture	3
8.	EC668	Low Power VLSI circuits	3
9.	EC669	VLSI Digital Signal Processing Systems	3
10.	EC670	Asynchronous System Design	3
11.	EC671	Advanced Digital Design	3
12.	EC672	Physical Design Automation	3
13.	EC673	Mixed - Signal Circuit Design	3

14.	EC674	Electronic packaging	3
15.	EC675	RF circuits	3
16.	EC676	Thermal Design of Electronic Equipment	3
17.	EC677	Functional Verification using Hardware Verification Languages	3
18.	EC678	Testability of Analog / Mixed-Signal Circuits & High Speed Circuit Design	3
19.	EC679	High Speed System Design	3
20.	EC612	DSP Architecture	3
21.	EC613	High Speed Communication Networks	3
22.	EC615	Digital Image Processing	3
23.	EC616	RF MEMS	3
24.	EC626	Bio MEMS	3

LIST OF OPEN ELECTIVES

Sl. No.	Course Code	Course Title	Credits
1.	EC653	Basics of VLSI	3
2.	EC662	Modeling and Synthesis with Verilog HDL	3

Course Code	**:**	**MA617**
Course Title	**:**	**Graph Theory and Discrete Optimization**
Number of Credits	**:**	**3**
Course Type	**:**	**Core**

Course Learning Objective

- To introduce the basics of graphs and combinatory required for VLSI design and Optimization.

Course Content

Basic definitions, Degree of vertices, Complement of a graph. Self complementary graph, some eccentricity properties of graphs. Tree, spanning tree. Directed graphs standard definitions; strongly, weakly, unilaterally connected digraphs, deadlock communication network. Matrix representation of graph and digraphs. Some properties (proof not expected).
Eulerian graphs and standard results relating to characterization. Hamiltonian graph-standard theorems (Dirac theorem, Chavathal theorem, closure of graph).Non Hamiltonian graph with maximum number of edges. Self-centered graphs and related simple theorems. Chromatic number; Vertex and edge (only properties and examples)-application to colouring. Planar graphs, Euler's formula, maximum number of edges in a planar graph. Five colour theorem.
DFS-BFS algorithm, shortest path algorithm, min-spanning tree and max-spanning tree algorithm, planarity algorithm. Matching theory, maximal matching and algorithms for maximal matching. Perfect matching (only properties and applications to regular graphs).
Flows in graphs, Ranking of participants in tournaments, simple properties and theorems on strongly connected tournaments. Application of Eulerian digraphs. PERT-CPM. Complexity of algorithms; P-NP-NPC-NP hard problems and examples.
Linear- Integer Linear programming, Conversion of TSP, maxflow, Knapsack scheduling, shortest path problems for Linear programming types - branch bound method to solve Knapsack problems- critical path and linear programming conversion- Floor shop scheduling problem- Personal assignment problem.
Dynamic programming- TSP- compartment problems- Best investment problems.

Text Books

1. *C. Papadimitriou & K. Steiglitz, "Combinatorial Optimization", Prentice Hall, 1982.*
2. *H. Gerez, "Algorithms for VLSI Design Automation", John Wiley, 1999.*

Reference Book

1. *B. Korte &J. Vygen, "Combinatorial Optimization", Springer- Verlag, 2000.*
2. *Recent literature in Graph Theory and Discrete Optimization.*

Course outcomes

At the end of the course student will be able

CO1: understand the various types of graph Algorithms and graph theory properties.

CO2: analyse the NP – complete problems.

CO3: distinguish the features of the various tree and matching algorithms

CO4: appreciate the applications of digraphs and graph flow.

CO5: understand the linear programming principles and its conversion.

Course Code	**:**	**EC651**
Course Title	**:**	**Analog IC Design**
Number of Credits	**:**	**3**
Course Type	**:**	**Core**

Course Learning Objectives

- To develop the ability design and analyze MOS based Analog VLSI circuits to draw the equivalent circuits of MOS based Analog VLSI and analyze their performance.
- To develop the skills to design analog VLSI circuits for a given specification.

Course Content

Basic MOS Device Physics – General Considerations, MOS I/V Characteristics, Second Order effects, MOS Device models. Short Channel Effects and Device Models. Single Stage Amplifiers – Basic Concepts, Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage.

Differential Amplifiers – Single Ended and Differential Operation, Basic Differential Pair, Common-Mode Response, Differential Pair with MOS loads, Gilbert Cell. Passive and Active Current Mirrors – Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors.

Frequency Response of Amplifiers – General Considerations, Common Source Stage, Source Followers, Common Gate Stage, Cascode Stage, Differential Pair. Noise – Types of Noise, Representation of Noise in circuits, Noise in single stage amplifiers, Noise in Differential Pairs.

Feedback Amplifiers – General Considerations, Feedback Topologies, Effect of Loading. Operational Amplifiers – General Considerations, One Stage Op Amps, Two Stage Op Amps, Gain Boosting, Common – Mode Feedback, Input Range limitations, Slew Rate, Power Supply Rejection, Noise in Op Amps. Stability and Frequency Compensation.

Bandgap References, Introduction to Switched Capacitor Circuits, Nonlinearity and Mismatch.

Text Books

1. *B.Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill Edition 2002.*
2. *Paul. R.Gray, Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley, (4/e), 2001.*

Reference Books

1. *D. A. Johns and K. Martin, "Analog Integrated Circuit Design", Wiley, 1997.*
2. *R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", Wiley, (3/e), 2010.*
3. *P.E.Allen, D.R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, 2002.*
4. *Recent literature in Analog IC Design.*

Course outcomes

At the end of the course student will be able

CO1: draw the equivalent circuits of MOS based Analog VLSI and analyze their performance.

CO2: design analog VLSI circuits for a given specification.

CO3: analyse the frequency response of the different configurations of a amplifier.

CO4: understand the feedback topologies involved in the amplifier design.

CO5: appreciate the design features of the differential amplifiers.

Course Code	**:**	**EC653**
Course Title	**:**	**Basics of VLSI**
Number of Credits	**:**	**3**
Course Type	**:**	**Core**

Course Learning Objectives

- To provide rigorous foundation in MOS and CMOS digital circuits
- To train the students in transistor budgets, clock speeds and the growing challenges of power consumption and productivity

Course Content

Introduction to CMOS circuits: MOS transistors, CMOS combinational logic gates, multiplexers, latches and flip-flops, CMOS fabrication and layout, VLSI design flow.

MOS transistor theory: Ideal I-V and C-V characteristics, non ideal I-V effects, DC transfer characteristics, Switch level RC delay models.

CMOS technologies: Layout design rules, CMOS process enhancement, Technology related CAD issues.

Circuit characterization and performance estimation: Delay estimation, Logical effort and transistor sizing, Power dissipation, Interconnect design margin, Reliability, Scaling.

Combinational circuit design: Static CMOS, Ratioed circuits, Cascode voltage switch logic, Dynamic circuits, Pass transistor circuits.

Text Books

1. *N.H.E.Weste, D. Harris, "CMOS VLSI Design (3/e)", Pearson, 2005.*
2. *J.Rabey, M. Pedram," Digital Integrated circuits (2/e)", PHI, 2003.*

Reference Book

1. *Pucknell & Eshraghian, "Basic VLSI Design", (3/e), PHI, 1996.*
2. *Recent literature in Basics of VLSI.*

Course outcomes

At the end of the course student will be able

CO1: implement the logic circuits using MOS and CMOS technology.
CO2: analyse various circuit configurations and their applications
CO3: analyse the merits of circuits according to the technology and applications change.
CO4: design low power CMOS VLSI circuits.
CO5: understand the rapid advances in CMOS Technology

Course Code	**:**	**EC655**
Course Title	**:**	**HDL Programming Laboratory**
Number of Credits	**:**	**2**
Course Type	**:**	**Laboratory**

List of Experiments

1. Adder/ Subtractor
2. Multiplexer/ Demultiplexer
3. Encoder/ Priority Encoder
4. Code Converter
5. Flipflop
6. Shift Register/ Universal Shift Register
7. Comparator
8. Upcounter/ Downcounter
9. Udps
10. Memory – ROM, RAM
11. Array Multiplier/ Array Multiplier With Pipelining
12. Fir Filter/ Fir Filter With Pipelinig

Course Code	**:**	**EC652**
Course Title	**:**	**VLSI System Testing**
Number of Credits	**:**	**3**
Course Type	**:**	**Core**

Course Learning Objectives

- To expose the students, the basics of testing techniques for VLSI circuits and Test Economics.

Course Content

Basics of Testing: Fault models, Combinational logic and fault simulation, Test generation for Combinational Circuits. Current sensing based testing. Classification of sequential ATPG methods. Fault collapsing and simulation

Universal test sets: Pseudo-exhaustive and iterative logic array testing. Clocking schemes for delay fault testing. Testability classifications for path delay faults. Test generation and fault simulation for path and gate delay faults.

CMOS testing: Testing of static and dynamic circuits. Fault diagnosis: Fault models for diagnosis, Cause-effect diagnosis, Effect-cause diagnosis.

Design for testability: Scan design, Partial scan, use of scan chains, boundary scan, DFT for other test objectives, Memory Testing.

Built-in self-test: Pattern Generators, Estimation of test length, Test points to improve testability, Analysis of aliasing in linear compression, BIST methodologies, BIST for delay fault testing.

Text Books

1. *N. Jha & S.D. Gupta, "Testing of Digital Systems", Cambridge, 2003.*
2. *W. W. Wen, "VLSI Test Principles and Architectures Design for Testability", Morgan Kaufmann Publishers. 2006*

Reference Books

1. *Michael L. Bushnell &Vishwani D. Agrawal," Essentials of Electronic Testing for Digital, memory & Mixed signal VLSI Circuits", Kluwar Academic Publishers. 2000.*
2. *P. K. Lala," Digital circuit Testing and Testability", Academic Press. 1997.*
3. *M. Abramovici, M. A. Breuer, and A.D. Friedman, "Digital System Testing and Testable Design", Computer Science Press, 1990.*
4. *Recent literature in VLSI System Testing.*

Course outcomes

At the end of the course student will be able

CO1: apply the concepts in testing which can help them design a better yield in IC design.

CO2: tackle the problems associated with testing of semiconductor circuits at earlier design levels so as to significantly reduce the testing costs.

CO3: analyse the various test generation methods for static & dynamic CMOS circuits.

CO4: identify the design for testability methods for combinational & sequential CMOS circuits.

CO5: recognize the BIST techniques for improving testability.

Course Code	**:**	**EC654**
Course Title	**:**	**Electronic Design Automation Tools**
Number of Credits	**:**	**3**
Course Type	**:**	**Core**

Course Learning Objectives

- To make the students exposed to Front end and Back end VLSI CAD tools.

Course Content

OS Architecture: System settings and configuration. Introduction to UNIX commandsHandling directories, Filters and Piping, Wildcards and Regular expression, Power Filters and Files Redirection. Working on Vi editor, Basic Shell Programming, TCL Scripting language.

Algorithms in VLSI:Partitioning methods: K-L, FM, and Simulated annealing algorithms.Placement and Routing algorithms, Interconnects and delay estimation.

Synthesis and simulation using HDLs-Logic synthesis using Verilog. Memory and FSM synthesis. Performance driven synthesis, Simulation- Types of simulation. Static timing analysis. Formal verification. Switch level and transistor level simulation. System Verilog- Introduction, Design hierarchy, Data types, Operators and language constructs. Functional coverage, Assertions, Interfaces and test bench structures.

Analog/Mixed Signal Modelling and Verification: Analog/Mixed signal modelling using Verilog-A and Verilog-AMS. Event Driven Modelling: Real number modelling of Analog/Mixed blocks modelling using Verilog-RNM/System Verilog. Analog/Digital Boundary Issues: boundary issues coverage

Text Books

1. *M.J.S.Smith, "Application Specific Integrated Circuits", Pearson, 2008.*
2. *S.Sutherland, S. Davidmann, P. Flake, "System Verilog For Design",(2/e), Springer,2006.*

Reference Books

1. *H.Gerez, "Algorithms for VLSI Design Automation", John Wiley, 1999*
2. *Z. Dr Mark, "Digital System Design with System Verilog ", Pearson, 2010.*
3. *Recent literature in Electronic Design Automation Tools.*

Course outcomes

At the end of the course student will be able

CO1: execute the special features of VLSI back end and front end CAD tools and UNIX shell script

CO2: explain the algorithms used for ASIC construction

CO3: design synthesizable Verilog and VHDL code.

CO4: explain the difference between Verilog and system Verilog and are able to write system Verilog code.

CO5: Model Analog and Mixed signal blocks using Verilog A and Verilog AMS

Course Code	**:**	**EC656**
Course Title	**:**	**Design of ASICs**
Number of Credits	**:**	**3**
Course Type	**:**	**Core**

Course Learning Objectives

- To prepare the student to be an entry-level industrial standard ASIC or FPGA designer.
- To give the student an understanding of issues and tools related to ASIC/FPGA design and implementation.
- To give the student an understanding of basics of System on Chip and Platform based design.
- To give the student an understanding of High performance algorithms

Course Content

Introduction to Technology, Types of ASICs, VLSI Design flow, Design and Layout Rules, Programmable ASICs - Antifuse, SRAM, EPROM, EEPROM based ASICs. Programmable ASIC logic cells and I/O cells. Programmable interconnects. Advanced FPGAs and CPLDs and Soft-core processors.

ASIC physical design issues, System Partitioning, Floorplanning and Placement. Algorithms: K-L, FM, Simulated annealing algorithms. Full Custom Design: Basics, Needs & Applications. Schematic and layout basics, Full Custom Design Flow.

Semicustom Approach: Synthesis (RTL to GATE netlist) - Introduction to Constraints (SDC), Introduction to Static Timing Analysis (STA). Place and Route (Logical to Physical Implementation): Floorplan and Power-Plan, Placement, Clock Tree Synthesis (clock planning), Routing, Timing Optimization, GDS generation.

Extraction, Logical equivalence and STA: Parasitic Extraction Flow, STA: Timing Flow, LEC: Introduction, flow and Tools used. Physical Verification: Introduction, DRC, LVS and basics of DFM.

System-On-Chip Design - SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures. High performance algorithms for ASICs/ SoCs as case studies – Canonic Signed Digit Arithmetic, KCM, Distributed Arithmetic, High performance digital filters for sigma-delta ADC.

Text Book

1. *M.J.S. Smith : Application Specific Integrated Circuits, Pearson, 2003*
2. *Sudeep Pasricha and NikilDutt, On-Chip Communication Architectures System on Chip Interconnect, Elsevier, 2008*

Reference Books

1. *H.Gerez, Algorithms for VLSI Design Automation, John Wiley, 1999*
2. *Jan.M.Rabaey et al, Digital Integrated Circuit Design Perspective (2/e), PHI 2003*
3. *David A.Hodges, Analysis and Design of Digital Integrated Circuits (3/e), MGH 2004*

4. *Hoi-Jun Yoo, Kangmin Leeand Jun Kyong Kim, Low-Power NoC for High-Performance SoC Design, CRC Press, 2008*
5. *An Integrated Formal Verification solution DSM sign-off market trends, www.cadence.com.*
6. *Recent literature in Design of ASICs.*

Course outcomes

At the end of the course student will be able

CO1: demonstrate VLSI tool-flow and appreciate FPGA and CPLD architectures
CO2: understand the issues involved in ASIC design, including technology choice, design management and tool-flow.
CO3: understand the algorithms used for ASIC construction.
CO4: understand Full Custom Design Flow and Tool used
CO5: understand Semicustom Design Flow and Tool used - from RTL to GDS and Logical to Physical Implementation
CO6: understand about STA, LEC, DRC, LVS, DFM
CO7: understand the basics of System on Chip and on chip communication architectures appreciate high performance algorithms for ASICs

Course Code	**:**	**EC658**
Course Title	**:**	**Analog IC Design Laboratory**
Number of Credits	**:**	**2**
Course Type	**:**	**Laboratory**

List of Experiments

1. Characteristics of NMOS & PMOS Transistor
2. Design of Common Source Amplifier with different Loads
3. Design of Common Gate Amplifier
4. Design of Common Drain Amplifier
5. Design of Single stage Cascode Amplifiers
6. Design of Current Mirrors
7. Design of Differential Amplifiers with Different Loads
8. Design of Two stage Opamp
9. Design of Telescopic Cascode Opamp
10. Design of Folded Cascode Opamp

Course Code	**:**	**EC 660**
Course Title	**:**	**ASIC – CAD Laboratory**
Number of Credits	**:**	**2**
Course Type	**:**	**Laboratory**

List of Experiments

1. Adder/ Subtractor
2. Multiplexer/ Demultiplexer
3. 8-bit Counter
4. Signed Pipelined Multiplier
5. Accumulator
6. MAC
7. Memory

The above experiments are carried out using the following tools:

1. Model SIM
2. Cadence
3. Synopsis
4. Mentor Graphics
5. Xilinx Planahead

Course Code	**:**	**EC661**
Course Title	**:**	**Digital System Design**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To get an idea about designing complex, high speed digital systems and how to implement such design.

Course Content

Mapping algorithms into Architectures: Data path synthesis, control structures, critical path and worst case timing analysis. FSM and Hazards.

Combinational network delay. Power and energy optimization in combinational logic circuit. Sequential machine design styles. Rules for clocking. Performance analysis.

Sequencing static circuits. Circuit design of latches and flip-flops. Static sequencing element methodology. Sequencing dynamic circuits. Synchronizers.

Data path and array subsystems: Addition / Subtraction, Comparators, counters, coding, multiplication and division. SRAM, DRAM, ROM, serial access memory, context addressable memory.

Reconfigurable Computing- Fine grain and Coarse grain architectures, Configuration architectures-Single context, Multi context, partially reconfigurable, Pipeline reconfigurable, Block Configurable, Parallel processing.

Text Books

1. *N.H.E.Weste, D. Harris, "CMOS VLSI Design (3/e)", Pearson, 2005.*
2. *W.Wolf, "FPGA- based System Design", Pearson, 2004.*
3. *S.Hauck, A.DeHon, "Reconfigurable computing: the theory and practice of FPGA-based computation", Elsevier, 2008.*

Reference Books

1. *F.P. Prosser, D. E. Winkel, "Art of Digital Design", 1987.*
2. *R.F.Tinde, "Engineering Digital Design", (2/e), Academic Press, 2000.*
3. *C. Bobda, "Introduction to reconfigurable computing", Springer, 2007.*
4. *M.Gokhale, P.S.Graham, "Reconfigurable computing: accelerating computation with field-programmable gate arrays", Springer, 2005.*
5. *C.Roth," Fundamentals of Digital Logic Design", Jaico Publishers, V ed., 2009.*
6. *Recent literature in Digital System Design.*

Course outcomes

At the end of the course student will be able

CO1: identify mapping algorithms into architectures.
CO2: summarize various delays in combinational circuit and its optimization methods.
CO3: summarize circuit design of latches and flip-flops.
CO4: construct combinational and sequential circuits of medium complexity that is based on VLSIs, and programmable logic devices.
CO5: summarize the advanced topics such as reconfigurable computing, partially reconfigurable, Pipeline reconfigurable architectures and block configurable.

Course Code	**:**	**EC662**
Course Title	**:**	**Modeling and Synthesis with Verilog HDL**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To design combinational, sequential circuits using Verilog HDL.
- To understand behavioral and RTL modeling of digital circuits
- To verify that a design meets its timing constraints, both manually and through the use of computer aided design tools
- To simulate, synthesize, and program their designs on a development board
- To verify and design the digital circuit by means of Computer Aided Engineering tools which involves in programming with the help of Verilog HDL.

Course Content

Hardware modeling with the verilog HDL. Encapsulation, modeling primitives, different types of description.

Logic system, data types and operators for modeling in verilog HDL. Verilog Models of propagation delay and net delay path delays and simulation, inertial delay effects and pulse rejection.

Behavioral descriptions in verilog HDL.Synthesis of combinational logic.

HDL-based synthesis - technology-independent design, styles for synthesis of combinational and sequential logic, synthesis of finite state machines, synthesis of gated clocks, design partitions and hierarchical structures.

Synthesis of language constructs, nets, register variables, expressions and operators, assignments and compiler directives. Switch-level models in verilog. Design examples in verilog.

Text Books

1. *M.D.Ciletti, "Modeling, Synthesis and Rapid Prototyping with the Verilog HDL", PHI, 1999.*
2. *S. Palnitkar, "Verilog HDL – A Guide to Digital Design and Synthesis", Pearson, 2003.*

Reference Books

1. *J Bhaskar, "A Verilog HDL Primer (3/e)", Kluwer, 2005.*
2. *M.G.Arnold, "Verilog Digital – Computer Design", Prentice Hall (PTR), 1999.*
3. *Recent literature in Modeling and Synthesis with Verilog HDL.*

Course outcomes

At the end of the course student will be able

CO1: understand the basic concepts of verilog HDL

CO2: model digital systems in verilog HDL at different levels of abstraction

CO3: know the simulation techniques and test bench creation.

CO4: understand the design flow from simulation to synthesizable version

CO5: get an idea of the process of synthesis and post-synthesis

Course Code	**:**	**EC663**
Course Title	**:**	**Optimizations of Digital Signal Processing Structures for VLSI**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To understand the various VLSI architectures for digital signal processing.
- To know the techniques of critical path and algorithmic strength reduction in the filter structures.
- To enable students to design VLSI system with high speed and low power.
- To encourage students to develop a working knowledge of the central ideas of implementation of DSP algorithm with optimized hardware.

Course Content

An overview of DSP concepts, Pipelining of FIR filters. Parallel processing of FIR filters. Pipelining and parallel processing for low power, Combining Pipelining and Parallel Processing.

Transformation Techniques: Iteration bound, Retiming, Folding and Unfolding

Pipeline interleaving in digital filters. Pipelining and parallel processing for IIR filters. Low power IIR filter design using pipelining and parallel processing, Pipelined adaptive digital filters.

Algorithms for fast convolution: Cook-Toom Algorithm, Cyclic Convolution. Algorithmic strength reduction in filters and transforms: Parallel FIR Filters, DCT and inverse DCT, Parallel Architectures for Rank-Order Filters.

Synchronous pipelining and clocking styles, clock skew and clock distribution in bit level pipelined VLSI designs. Wave pipelining, constraint space diagram and degree of wave pipelining, Implementation of wave-pipelined systems, Asynchronous pipelining.

Text Book

1. *K.K.Parhi, VLSI Digital Signal Processing Systems, John-Wiley, 2007*

Reference Books

1. *U. Meyer -Baese, Digital Signal Processing with FPGAs, Springer, 2004*
2. *Wayne Burleson, Konstantinos Konstantinides, Teresa H. Meng, VLSI Signal Processing, 1996.*
3. *Richard J. Higgins, Digital signal processing in VLSI, 1990.*
4. *Sun Yuan Kung, Harper J. Whitehouse, VLSI and modern signal processing, 1985*
5. *Magdy A. Bayoumi, VLSI Design Methodologies for Digital Signal Processing, 2012*

6. *Earl E. Swartzlander*, *VLSI signal processing systems*, *1986*.
7. Recent literature in *Optimizations of Digital Signal Processing Structures for VLSI.*

Course outcomes

At the end of the course student will be able

CO1: understand the overview of DSP concepts and design architectures for DSP algorithms.
CO2: improve the overall performance of DSP system through various transformation and optimization techniques.
CO3: perform pipelining and parallel processing on FIR and IIR systems to achieve high speed and low power.
CO4: optimize design in terms of computation complexity and speed.
CO5: understand clock based issues and design asynchronous and wave pipelined systems.

Course Code	**:**	**EC664**
Course Title	**:**	**Cognitive Radio**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objective

- This subject introduces the fundamentals of multi rate signal processing and cognitive radio.

Course Content

Filter banks-uniform filter bank. Direct and DFT approaches. Introduction to ADSL Modem. Discrete multitone modulation and its realization using DFT. QMF. STFT. Computation of DWT using filter banks.

DDFS- ROM LUT approach. Spurious signals, jitter. Computation of special functions using CORDIC. Vector and rotation mode of CORDIC.CORDIC architectures.

Block diagram of a software radio. Digital down converters and demodulators Universal modulator and demodulator using CORDIC. Incoherent demodulation - digital approach for I and Q generation, special sampling schemes. CIC filters. Residue number system and high speed filters using RNS. Down conversion using discrete Hilbert transform. Under sampling receivers, Coherent demodulation schemes.

Concept of Cognitive Radio, Benefits of Using SDR, Problems Faced by SDR, Cognitive Networks, Cognitive Radio Architecture. Cognitive Radio Design, Cognitive Engine Design,

A Basic OFDM System Model, OFDM based cognitive radio, Cognitive OFDM Systems, MIMO channel estimation, Multi-band OFDM, MIMO-OFDM synchronization and frequency offset estimation. Spectrum sensing to detect Specific Primary System, Spectrum Sensing for Cognitive OFDMA Systems.

Text Books

1. *J. H. Reed, "Software Radio", Pearson, 2002.*
2. *U. Meyer – Baese, "Digital Signal Processing with FPGAs", Springer, 2004.*
3. *H. Arslan "Cognitive Radio, Software Defined Radio and Adaptive Wireless Systems", University of South Florida, USA, Springer, 2007.*

Reference Books

1. *S. K. Mitra, "Digital Signal processing", McGrawHill, 1998*
2. *K.C.Chen, R.Prasad, "Cognitive Radio Networks", Wiley, 2009-06-15.*
3. *T. W. Rondeau, C.W.Bostian, "Artificial Intelligence in Wireless Communications", 2009.*
4. *Tusi, "Digital Techniques for Wideband receivers", Artech House, 2001.*
5. *T. DarcChiueh, P. Yun Tsai," OFDM baseband receiver design for wireless communications", Wiley, 2007*
6. *Recent literature in Cognitive Radio.*

Course outcomes

At the end of the course student will be able

CO1: gain knowledge on multirate systems.
CO2: develop the ability to analyze, design, and implement any application using FPGA.
CO3: be aware of how signal processing concepts can be used for efficient FPGA based system design.
CO4: understand the rapid advances in Cognitive radio technologies.
CO5: explore DDFS, CORDIC and its application.

Course Code	**:**	**EC665**
Course Title	**:**	**VLSI Process Technology**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To provide rigorous foundation in MOS and CMOS fabrication process.

Course Content

Electron grade silicon. Crystal growth. Wafer preparation. Vapour phase and molecular beam epitaxy. SOI. Epitaxial evaluation. Oxidation techniques, systems and properties. Oxidation defects.

Optical, electron, X-ray and ion lithography methods. Plasma properties, size, control, etch mechanism, etch techniques and equipments.

Deposition process and methods. Diffusion in solids. Diffusion equation and diffusion mechanisms.

Ion implantation and metallization. Process simulation of ion implementation, diffusion, oxidation, epitaxy, lithography, etching and deposition. NMOS, CMOS, MOS memory and bipolar IC technologies. IC fabrication.

Analytical and assembly techniques. Packaging of VLSI devices.

Text Books

1. *S.M.Sze, "VLSI Technology (2/e)" , McGraw Hill, 1988*
2. *W. Wolf, "Modern VLSI Design", (3/e), Pearson,2002*

Course outcomes

At the end of the course student will be able

CO1: appreciate the various techniques involved in the VLSI fabrication process.
CO2: understand the different lithography methods and etching process.
CO3: appreciate the deposition and diffusion mechanisms.
CO4: analyze the fabrication of NMOS, CMOS memory and bipolar devices
CO5: understand the nuances of assembly and packaging of VLSI devices.

Course Code	**:**	**EC666**
Course Title	**:**	**Analysis and Design of Digital Systems using VHDL**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To prepare the student to understand the VHDL language feature to realize the complex digital systems.
- To design and simulate sequential and concurrent techniques in VHDL
- To explain modeling of digital systems using VHDL and design methodology
- To explain predefined attributes and configurations of VHDL.
- To Understand behavioral, non-synthesizable VHDL and its role in modern design

Course Content

An overview of design procedures for system design using CAD tools. Design verification tools. Examples using commercial PC based VLSI CAD tools. Design methodology based on VHDL. Basic concepts and structural descriptions in VHDL.

Characterizing hardware languages, objects and classes, signal assignments, concurrent and sequential assignments. Structural specification of hardware.

Design organization, parameterization and high level utilities, definition and usage of subprograms, packaging parts and utilities, design parameterization, design configuration, design libraries. Utilities for high-level descriptions.

Data flow and behavioral description in VHDL- multiplexing and data selection, state machine description, open collector gates, three state bussing, general dataflow circuit, updating basic utilities. Behavioral description of hardware.

CPU modeling for discrete design- Parwan CPU, behavioral description, bussing structure, data flow, test bench, a more realistic Parwan. Interface design and modeling. VHDL as a modeling language.

Text Books

1. *Z.Navabi, "VHDL Analysis and Modeling of Digital Systems", (2/e), McGraw Hill, 1998.*
2. *Perry, "VHDL (3/e)", McGraw Hill.2002*

Reference Books

1. *A. Dewey, "Analysis and Design of Digital Systems with VHDL", CL-Engineering, 1996.*
2. *Z.Navabi,"VHDL: modular design and synthesis of cores and systems", McGraw, 2007.*
3. *C. H. Roth, Jr., L.K.John, "Digital Systems Design Using VHDL - Thomson Learning EMEA", Limited, 2008.*
4. *Recent literature in Analysis and Design of Digital Systems using VHDL.*

Course outcomes

At the end of the course student will be able

CO1: model, simulate, verify, and synthesize with hardware description languages.
CO2: understand and use major syntactic elements of VHDL - entities, architectures, processes, functions, common concurrent statements, and common sequential statements
CO3: design digital logic circuits in different types of modeling
CO4: demonstrate timing and resource usage associated with modeling approach.
CO5: use computer-aided design tools for design of complex digital logic circuits.

Course Code	**:**	**EC667**
Course Title	**:**	**Advanced Computer Architecture**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To give an exposure on look ahead pipelining- parallelism, multiprocessor scheduling, multithreading and various memory organizations.

Course Content

Multiprocessors and multi-computers. Multi-vector and SIMD computers. PRAM and VLSI Models. Conditions of parallelism. Program partitioning and scheduling. Program flow mechanisms. Parallel processing applications. Speed up performance law.
Advanced processor technology. Superscalar and vector processors. Memory hierarchy technology. Virtual memory technology. Cache memory organization. Shared memory organization.
Linear pipeline processors. Non linear pipeline processors. Instruction pipeline design. Arithmetic design. Superscalar and super pipeline design. Multiprocessor system interconnects. Message passing mechanisms.
Vector Processing principle. Multivector multiprocessors. .Compound Vector processing. Principles of multithreading. Fine grain multicomputer. Scalable and multithread architectures. Dataflow and hybrid architectures.
Parallel programming models. Parallel languages and compilers. Parallel programming environments. Synchronization and multiprocessing modes. Message passing program development. Mapping programs onto multicomputer. Multiprocessor UNIX design goals. MACH/OS kernel architecture. OSF/1 architecture and applications.

Text Books

1. *K. Hwang, "Advanced Computer Architecture ", Tata McGraw Hill, 2001.*
2. *W. Stallings," Computer Organization and Architecture", McMillan, 1990.*

Reference Book

1. *M.J. Quinn, "Designing Efficient Algorithms for Parallel Computer', McGraw Hill, 1994.*
2. *Recent literature in Advanced Computer Architecture.*

Course outcomes

At the end of the course student will be able

CO1: apply the basic knowledge of partitioning and scheduling in Multiprocessors.

CO2: analyze and design cache memory, virtual memory and shared memory Organizations.

CO3: distinguish and analyze the design properties of Linear and Non - Linear processors.

CO4: analyze the principles of multithreading in hybrid Architectures.

CO5: write any parallel programming models for various architectures and Applications.

Course Code	**:**	**EC668**
Course Title	**:**	**Low Power VLSI Circuits**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To expose the students to the low voltage device modeling, low voltage, low power VLSI CMOS circuit design.

Course Content

Evolution of CMOS technology.0.25 µm and 0.1 µm technologies. Shallow trench isolation. Lightly-doped drain. Buried channel. BiCMOS and SOI CMOS technologies. Second order effects and capacitance of MOS devices.

CMOS inverters, static logic circuits of CMOS, pass transistor, BiCMOS, SOI CMOS and low power CMOS techniques.

Basic concepts of dynamic logic circuits. Various problems associated with dynamic logic circuits. Differential, BiCMOS and low voltage dynamic logic circuits.

Different types of memory circuits.

Adder circuits, Multipliers and advanced structures – PLA, PLL, DLL and processing unit.

Text Books

1. *J.Rabaey, "Low Power Design Essentials (Integrated Circuits and Systems)", Springer, 2009*
2. *J.B.Kuo&J.H.Lou, "Low-voltage CMOS VLSI Circuits", Wiley, 1999.*

Reference Books

1. *A.Bellaowar & M.I.Elmasry,"Low power Digital VLSI Design, Circuits and Systems", Kluwer, 1996.*
2. *Recent literature in Low Power VLSI Circuits.*

Course outcomes

At the end of the course student will be able

CO1: acquire the knowledge about various CMOS fabrication process and its modeling.
CO2: infer about the second order effects of MOS transistor characteristics.
CO3: analyze and implement various CMOS static logic circuits.
CO4: learn the design of various CMOS dynamic logic circuits.
CO5: learn the design techniques low voltage and low power CMOS circuits for various applications.
CO6: learn the different types of memory circuits and their design.
CO7: design and implementation of various structures for low power applications.

Course Code	**:**	**EC669**
Course Title	**:**	**VLSI Digital Signal Processing Systems**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To enable students to design VLSI systems with high speed and low power.
- To encourage students to develop a working knowledge of the central ideas of implementation of DSP algorithm with optimized hardware.

Course Content

An overview of DSP concepts, Representations of DSP algorithms. Systolic Architecture Design: FIR Systolic Array, Matrix-Matrix Multiplication, 2D Systolic Array Design. Digital Lattice Filter Structures: Schur Algorithm, Derivation of One-Multiplier Lattice Filter, Normalised Lattice Filter, Pipelining of Lattice Filter.

Scaling and Round off Noise - State variable description of digital filters, Scaling and Round off Noise computation, Round off Noise in Pipelined IIR Filters, Round off Noise Computation using state variable description, Slow-down, Retiming and Pipelining.

Bit level arithmetic Architectures- parallel multipliers, interleaved floor-plan and bit-plane-based digital filters, Bit serial multipliers, Bit serial filter design and implementation, Canonic signed digit arithmetic, Distributed arithmetic.

Redundant arithmetic -Redundant number representations, carry free radix-2 addition and subtraction, Hybrid radix-4 addition, Radix-2 hybrid redundant multiplication architectures, data format conversion, Redundant to Non-redundant converter.

Numerical Strength Reduction - Subexpression Elimination, Multiple Constant Multiplication, Subexpression Sharing in Digital Filters, Additive and Multiplicative Number Splitting.

Text Book

1. *K.K.Parhi, "VLSI Digital Signal Processing Systems", John-Wiley, 2007.*

Reference Book

1. *U. Meyer -Baese, Digital Signal Processing with FPGAs, Springer, 2004.*
2. *Recent literature in VLSI Digital Signal Processing Systems.*

Course outcomes

At the end of the course student will be able

CO1: Acquire the knowledge of round off noise computation and numerical strength reduction.
CO2: Ability to design Bit level and redundant arithmetic Architectures.

Course Code	**:**	**EC670**
Course Title	**:**	**Asynchronous System Design**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- This subject introduces the fundamentals and performance of Asynchronous system
- To familiarize the dependency graphical analysis of signal transmission graphs
- To learn software languages and its syntax and operations for implementing Asynchronous Designs

Course Content

Fundamentals: Handshake protocols, Muller C-element, Muller pipeline, Circuit implementation styles, theory. Static data-flow structures: Pipelines and rings, Building blocks, examples

Performance: A quantitative view of performance, quantifying performance, Dependency graphic analysis. Handshake circuit implementation: Fork, join, and merge, Functional blocks, mutual exclusion, arbitration and metastability.

Speed-independent control circuits: Signal Transition graphs, Basic Synthesis Procedure, Implementation using state-holding gates, Summary of the synthesis Process, Design examples using Petrify. Advanced 4-phase bundled data protocols and circuits: Channels and protocols, Static type checking, more advanced latch control circuits.

High-level languages and tools: Concurrency and message passing in CSP, Tangram program examples, Tangram syntax-directed compilation, Martin's translation process, Using VHDL for Asynchronous Design. An Introduction to Balsa: Basic concepts, Tool set and design flow, Ancillary Balsa Tools

The Balsa language: Data types, Control flow and commands, Binary/Unary operators, Program structure. Building library Components: Parameterized descriptions, Recursive definitions. A simple DMA controller: Global Registers, Channel Registers, DMA control structure, The Balsa description.

Text Books

1. *Asynchronous Circuit Design- Chris. J. Myers, John Wiley & Sons, 2001.*
2. *Handshake Circuits An Asynchronous architecture for VLSI programming – Kees Van Berkel Cambridge University Press, 2004*

Reference Books

1. *Principles of Asynchronous Circuit Design-Jens Sparso, Steve Furber, Kluver Academic Publishers, 2001.*
2. *Asynchronous Sequential Machine Design and Analysis, Richard F. Tinder, 2009*

3. *A Designer's Guide to Asynchronous VLSI, Peter A. Beerel, Recep O. Ozdag, Marcos Ferretti, 2010*
4. *Recent literature in Asynchronous System Design.*

Course outcomes

At the end of the course student will be able

CO1: understand the fundamentals of Asynchronous protocols

CO2: analyse the performance of Asynchronous System and implement handshake circuits

CO3: understand the various control circuits and Asynchronous system modules

CO4: gain the experience in using high level languages and tools for Asynchronous Design

CO5: learn commands and control flow of Balsa language for implementing Asynchronous Designs

Course Code	**:**	**EC671**
Course Title	**:**	**Advanced Digital Design**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To make the students learn about graphical models and state diagram in designing optimized digital circuits.
- To provide the students a detailed knowledge of scheduling algorithm, synthesis of pipelined circuits and scheduling pipelined circuits
- To enable the students to design digital design with advanced technique like Sequential logic optimization and test the designed circuit Testability considerations.

Course Content

Different types of graphs. Combinational optimization- Graph optimization problems and algorithms. Boolean functions, statisfiability and cover. Abstract models, state diagrams. Data flow and sequencing graphs , compilation and behavioural optimization.

Architectural synthesis - Circuit specifications for architectural synthesis . Temporal domain, spatial domain , hierarchical models. Synchronization problems . Area and performance estimation. Strategies for architectural optimization, Data path synthesis of pipelined circuits.

Scheduling algorithms-Scheduling with and without constraints. Scheduling algorithms for extended sequencing models. Scheduling pipelined circuits.

Resource sharing and binding. Sharing and binding for resource dominated circuits and general circuits. Concurrent binding and scheduling. Resource sharing and binding for non-scheduled sequencing graphs.

Sequential logic optimization-sequential circuit optimization using state based models and network models. Implicit finite state machine. Traversal methods. Testability considerations for synchronous circuits.

Text Books

1. *G.De Micheli, "Synthesis and optimization of Digital circuits", McGraw Hill,1994 .*
2. *C. Roth, "Fundamentals of Digital Logic Design", Jaico Publishers, V ed., 2009.*
3. *Balabanian, "Digital Logic Design Principles", Wiley publication, 2000.*

Reference Books

1. *J. F. Wakerly,"Digital Design principles and practices", 3rd edition, PHI publication, 1999.*
2. *S.Brown, "Fundamentals of digital logic", Tata McGraw Hill publication, 2007.*
3. *N. N. Biswas, "Logic Design Theory", Prentice Hall of India, 2001.*

4. *John M Yarbrough, "Digital Logic applications and Design", Thomson Learning, 2001*.
5. *Recent literature in Advanced Digital Design.*

Course outcomes

At the end of the course student will be able

CO1: understand advanced state of art techniques of digital design.

CO2: synthesis the circuits and evaluate its performance in terms of area, power and speed.

CO3: understand the use of scheduling algorithm.

CO4: gain in-depth knowledge of sequential digital circuits designed using resource sharing.

CO5: understand synchronization across clock domains, timing analysis, and Testability considerations

Course Code	**:**	**EC672**
Course Title	**:**	**Physical Design Automation**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- Understand the concepts of Physical Design Process such as partitioning, Floorplanning, Placement and Routing.
- Discuss the concepts of design optimization algorithms and their application to physical design automation.
- Understand the concepts of simulation and synthesis in VLSI Design Automation
- Formulate CAD design problems using algorithmic methods

Course Content

VLSIdesign automation tools- algorithms and system design. Structural and logic design. Transistor level design. Layout design. Verification methods. Design management tools.

Layout compaction, placement and routing. Design rules, symbolic layout. Applications of compaction. Formulation methods. Algorithms for constrained graph compaction. Circuit representation. Wire length estimation. Placement algorithms. Partitioning algorithms.

Floor planning and routing- floor planning concepts. Shape functions and floor planning sizing. Local routing. Area routing. Channel routing, global routing and its algorithms.

Simulation and logic synthesis- gate level and switch level modeling and simulation. Introduction to combinational logic synthesis. ROBDD principles, implementation, construction and manipulation. Two level logic synthesis.

High-level synthesis- hardware model for high level synthesis. Internal representation of input algorithms. Allocation, assignment and scheduling. Scheduling algorithms. Aspects of assignment. High level transformations.

Text Books

1. *S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley ,1998.*
2. *N.A.Sherwani , "Algorithms for VLSI Physical Design Automation", (3/e), Kluwer,1999.*

Reference Books

1. *S.M. Sait , H. Youssef, "VLSI Physical Design Automation", World scientific, 1999.*
2. *M.Sarrafzadeh, "Introduction to VLSI Physical Design", McGraw Hill (IE), 1996*
3. *Recent literature in Physical Design Automation.*

Course outcomes

At the end of the course student will be able

CO1: Students are able to know how to place the blocks and how to partition the blocks while for designing the layout for IC.
CO2: Students are able to solve the performance issues in circuit layout.
CO3: Students are able to analyze physical design problems and Employ appropriate automation algorithms for partitioning, floor planning, placement and routing
CO4: Students are able to decompose large mapping problem into pieces, including logic optimization with partitioning, placement and routing
CO5: Students are able to analyze circuits using both analytical and CAD tools

Course Code	**:**	**EC673**
Course Title	**:**	**Mixed - Signal Circuit Design**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To make the students to understand the design and performance measures concept of mixed signal circuit.

Course Content

Concepts of Mixed-Signal Design and Performance Measures. Fundamentals of Data Converters. Nyquist Rate Converters and Over sampling Converters.

Design methodology for mixed signal IC design using gm/Id concept.

Design of Current mirrors. References. Comparators and Operational Amplifiers.

CMOS Digital Circuits Design: Design of MOSFET Switches and Switched-Capacitor Circuits, Layout Considerations.

Design of frequency and Q tunable continuous time filters.

Text Books

1. *R. Jacob Baker, Harry W. Li, David E. Boyce, CMOS, Circuit Design, Layout, and Simulation, Wiley-IEEE Press, 1998*
2. *David A. Johns and Ken Martin, Analog Integrated Circuit Design, John Wiley and Sons, 1997.*

Course outcomes

At the end of the course student will be able

CO1: appreciate the fundamentals of data converters and also optimized their performances.
CO2: understand the design methodology for mixed signal IC design using gm/Id concept.
CO3: analyze the design of current mirrors and operational amplifiers
CO4: design the CMOS digital circuits and implement its layout.
CO5: design the frequency and Q tunable time domain filters.

Course Code	**:**	**EC674**
Course Title	**:**	**Electronic Packaging**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To expose the students to all aspects of electronic packaging including electrical, thermal, mechanical and reliability issues.

Course Content

Functions of an Electronic Package, Packaging Hierarchy, IC packaging: MEMS packaging, consumer electronics packaging, medical electronics packaging, Trends, Challenges, Driving Forces on Packaging Technology, Materials for Microelectronic packaging, Packaging Material Properties, Ceramics, Polymers, and Metals in Packaging, Material for high density interconnect substrates

Electrical Anatomy of Systems Packaging, Signal Distribution, Power Distribution, Electromagnetic Interference, Design Process Electrical Design: Interconnect Capacitance, Resistance and Inductance fundamentals; Transmission Lines , Clock Distribution, Noise Sources, power Distribution, signal distribution, EMI, Digital and RF Issues. Processing Technologies, Thin Film deposition, Patterning, Metal to Metal joining.

IC Assembly – Purpose, Requirements, Technologies, Wire bonding, Tape Automated Bonding, Flip Chip, Wafer Level Packaging , reliability, wafer level burn – in and test.Single chip packaging : functions, types, materials processes, properties, characteristics, trends.Multi chip packaging : types, design, comparison, trends. Passives: discrete, integrated, embedded –encapsulation and sealing: fundamentals, requirements, materials, processes

Printed Circuit Board: Anatomy, CAD tools for PCB design, Standard fabrication, Microvia Boards. Board Assembly: Surface Mount Technology, Through Hole Technology, Process Control and Design challenges.Thermal Management, Heat transfer fundamentals, Thermal conductivity and resistance, Conduction, convection and radiation – Cooling requirements.

Reliability, Basic concepts, Environmental interactions. Thermal mismatch and fatigue – failures – thermo mechanically induced – electrically induced – chemically induced. Electrical Testing: System level electrical testing, Interconnection tests, Active Circuit Testing, Design for Testability.

Text Book

1. *Tummala, Rao R., Fundamentals of Microsystems Packaging, McGraw Hill, 2001*

Reference Books

1. *Blackwell (Ed), The electronic packaging handbook, CRC Press, 2000.*
2. *Tummala, Rao R, Microelectronics packaging handbook, McGraw Hill, 2008.*
3. *Bosshart, Printed Circuit Boards Design and Technology,TataMcGraw Hill, 1988.*

4. *R.G. Kaduskar and V.B.Baru, Electronic Product design, Wiley India, 2011*
5. *R.S.Khandpur, Printed Circuit Board, Tata McGraw Hill, 2005*
6. *Recent literature in Electronic Packaging*.

Course outcomes

At the end of the course student will be able

CO1: Design of PCBs which minimize the EMI and operate at higher frequency.
CO2: Enable design of packages which can withstand higher temperature, vibrations and shock.

Course Code	**:**	**EC675**
Course Title	**:**	**RF Circuits**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To impart knowledge on basics of IC design at RF frequencies.

Course Content

Characteristics of passive IC components at RF frequencies – interconnects, resistors, capacitors, inductors and transformers – Transmission lines. Noise – classical two-port noise theory, noise models for active and passive components

High frequency amplifier design – zeros as bandwidth enhancers, shunt-series amplifier, f_T doublers, neutralization and unilateralization

Low noise amplifier design – LNA topologies, power constrained noise optimization, linearity and large signal performance

Mixers – multiplier-based mixers, subsampling mixers, diode-ring mixers

RF power amplifiers – Class A, AB, B, C, D, E and F amplifiers, modulation of power amplifiers, linearity considerations

Oscillators & synthesizers – describing functions, resonators, negative resistance oscillators, synthesis with static moduli, synthesis with dithering moduli, combination synthesizers – phase noise considerations.

Text Books

1. *T.homas H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits", 2nd ed., Cambridge, UK: Cambridge University Press, 2004.*
2. *B.Razavi, "RF Microelectronics", 2nd Ed., Prentice Hall, 1998.*

Reference Books

1. *A. Abidi, P.R. Gray, and R.G. Meyer, eds., "Integrated Circuits for Wireless Communications", New York: IEEE Press, 1999.*
2. *R. Ludwig and P. Bretchko, "RF Circuit Design, Theory and Applications", Pearson, 2000.*
3. *Mattuck,A., "Introduction to Analysis", Prentice-Hall,1998.*
4. *Recent literature in RF Circuits.*

Course outcomes

At the end of the course student will be able

CO1: understand the Noise models for passive components and noise theory

CO2: analyse the design of a high frequency amplifier

CO3: appreciate the different LNA topologies & design techniques

CO4: distinguish between different types of mixers

CO5: analyse the various types of synthesizers, oscillators and their characteristics.

Course Code	**:**	**EC676**
Course Title	**:**	**Thermal Design of Electronic Equipment**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To expose the students to all aspects of electronic equipment and components including electrical, thermal, fluid dynamics and reliability issues.

Course Content

Packaging Levels, Package Function, Stages in the Development of a Packaging Technology.Packaging of Electronic Equipment, Components of Electronic Systems, Thermal management in electronic devices - Packaging Trends. Electronic packaging and interconnection technology.

Conduction in Electronic Equipment: Thermal Conductivity, Thermal Resistances, Conductivity in Solids, Conductivity in Fluids, Conduction—Steady State, Conduction in Simple Geometries, Conduction through a Plane Wall, Conduction through Cylinders and Spheres. Conduction—Transient, Lumped Capacitance Method, Conduction in Extended Surfaces. Fin Efficiency, Fin Optimization, Fin Surface Efficiency, Thermal Contact Resistance in Electronic Equipment, Discrete Heat Sources and Thermal Spreading.

Fluid Dynamics for Electronic Equipment- Boundary Layer Theory, Turbulent Flow, Loss Coefficients and Dynamic Drag, Fans and Pumps, Electronic Chassis Flow. Convection Heat Transfer in Electronic Equipment.Natural Convection in Electronic Devices, Overall Heat Transfer Coefficient.Liquid Cooling Systems, Coolant Selection, Pressure Drop and Pump Requirements.Air Cooling System, Induced or Draft Cooling, Selection of Fans and Blowers.

Radiation Heat Transfer in Electronic Equipment, The Electromagnetic Spectrum, Radiation Equations , Stefan-Boltzmann Law, Surface Characteristics, Emittance, Emittance Factor, Emittance from Extended Surface, Absorptance, Reflectance, Specular Reflectance, Heat Transfer with Phase Change. Combined Modes of Heat Transfer for Electronic Equipment, Radiation and Convection in Parallel.

Introduction to Thermal Design of Electronic Equipment. Analysis of Thermal Failure of Electronic Components. Analysis of Thermal Stresses and Strain, Effect of PCB Bending Stiffness on Wire Stresses, Vibration Fatigue in Lead Wires and Solder Joints. Electronics Cooling Methods in Industry. Heat Sinks, Heat Pipes, Heat Pipes in Electronics Cooling, Thermoelectric Cooling, Immersion Cooling, Cooling Techniques for High Density Electronics.

Reference Books

1. *Rao R. Tummala: Fundamentals of Microsystem Packaging, McGraw Hill, 2001.*
2. *Richard K. Ulrich &William D. Brown Advanced Electronic Packaging - 2nd Edition: IEEE Press, 1995.*
3. *Yunus A. Cengel: Heat Transfer – A Practical Approach, McGraw Hill, 2003.*
4. *Recent literature in Thermal Design of Electronic Equipment.*

Course outcomes

At the end of the course student will be able

CO1: design of electronic equipment which minimizes the thermal failures and get the knowledge on cooling Techniques.
CO2: design a package which can withstand higher temperature, vibrations and shock.
CO3: understand the fluid dynamics of electronic cooling systems and heat transfer mechanisms
CO4: appreciate the principle behind heat transfer equipments.
CO5: analyse of thermal stress and strain and cooling techniques.

Course Code	**:**	**EC677**
Course Title	**:**	**Functional Verification using Hardware Verification Languages**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

Course Content

System Verilog (SV) - Data Types, Arrays, Structures, Unions, Procedural Blocks, Tasks & Functions, Procedural Statements, Interfaces, Basic OOPs, Randomization, Threads & Inter Process Communication, Advanced OOPs & Test bench guidelines, Advanced Interfaces,

A Complete System Verilog Test Bench (SVTB), Functional Coverage in System Verilog, Interfacing with C, FSM Modeling with SV, Connecting Test bench & Design, Behavioral & Transaction Level Modeling with SV

System Verilog Assertions (SVA) – Introduction to SVA, Building blocks, Properties, Boolean expressions, Sequence, Single & Multiple Clock definitions, Implication operators (Overlapping & Non-overlapping), Repeatition operators, Built-in System functions ($past, $stable, $onehot, $onehot0, $isunknown), Constructs (ended, and, intersect, or, first_match, throughout, within, disableiff, expect, matched, if –else), assertion directives, nested implication, formal arguments in property,

SVA using local variables, calling subroutines, SVA for functional coverage, Connecting SVA to the Design or Test bench, SVA for FSMs, Memories, Protocol checkers, SVA Simulation Methodology, Assertions: Practice & Methodology, Re-use of Assertions, Tracking coverage with Assertions, Using SVA with other languages.

Functional Verification coverage using design, verification languages and implementation standards: Verilog IEEE 1364, VHDL IEEE 1076, System Verilog IEEE 1800, Property Specific Language (PSL) IEEE 1850, System C™ IEEE 1666, Encryption IEEE 1735, *e* Verification Language IEEE 1647, Open Verification Methodology (OVM) and Universal Verification Methodology (UVM).

Text Books

1. *SystemVerilog for design: a guide to using SystemVerilog for hardware design and modeling By Stuart Sutherland, Simon Davidmann, Peter Flake Edition: illustrated Published by Springer, 2004 ISBN 1402075308, 9781402075308*
2. *System Verilog for Verification: A Guide to Learning the Test bench Language Features By Chris Spear Edition: 2, Published by Springer, 2008 ISBN 0387765298, 9780387765297*

3. *A Practical guide for System Verilog Assertions By Srikanth Vijayaraghavan & Meyyappan Ramanathan Edition: illustrated Published by Springer, 2005 ISBN 0387260498, 9780387260495*
4. *The Art of Verification with System Verilog Assertions By Faisal I.Haque, Jonathan Michelson, Khizar A.Khan Published by Verification Central 2006 ISBN-13:978-0-9711994-1-5*
5. *System-on-a-Chip Verification: Methodology and Techniques by Prakash Rashinkar, Peter Paterson, Leena Singh and Published by Kluwer Academic Publishers 2004, New York, ISBN-0-306-46995-2.*

Reference Books

1. *Writing testbenches using System Verilog By Janick Bergeron Edition: illustrated Published by Birkhäuser, 2006 ISBN 0387292217, 9780387292212*
2. *SystemVerilog Assertions Handbook: --for Formal and Dynamic Verification - Ben Cohen, cohen, Venkataramanan, Kumari, Srinivasan Venkataramanan, Ajeetha Kumari - Published by vhdlcohen publishing, 2005 (ISBN 0970539479, 9780970539472).*
3. *An Integrated Formal Verification solution DSM sign-off market trends, www.cadence.com.*
4. *Recent literature in Functional Verification using Hardware Verification Languages.*

Course outcomes

At the end of the course student will be able

Course Code	**:**	**EC678**
Course Title	**:**	**Testability of Analog / Mixed-Signal Circuits & High Speed Circuit Design**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

Course Content

Overview of Mixed-signal Testing. DC and Parametric Measurements. DAC Testing: Basics of converter testing, Basic DC tests, Transfer curve tests, Dynamic DAC tests, DAC Architectures.

ADC Testing: ADC testing versus DAC testing, DC tests and Transfer curve tests, Dynamic ADC tests, ADC Architectures. **Sampling Theory. DSP based testing:** Advantages of DSP based testing, DSP, Discrete-time transforms, The Inverse FFT.

Analog Channel Testing. Fundamentals of RF Testing. Design for Test: Overview, Advantages of DFT, Digital Scan, Digital BIST, Digital DFT for Mixed-signal circuits, Mixed-signal boundary scan & BIST, Ad-hoc Mixed signal DFT, RF DFT.

High speed design techniques: High Speed Op-amps, High Speed op-amp applications, RF/IF Subsystems.

High Speed sampling and High Speed ADCs, High Speed DACs and DDS systems.

Text Books

1. *An Introduction to Mixed-signal IC test & Measurement - Mark Burns, Gordon W. Roberts*
2. *High Speed Design Techniques - Walt Kester, Analog Devices*

Reference Books

1. *Linda S. Milor, "A Tutorial Introduction to Research on Analog and Mixed-Signal Circuit Testing", IEEE Transactions on circuits and systems*-II: *Analog and Digital signal processing, Vol. 45, No. 10, October 1998.*
2. *The Fundamentals of Mixed Signal Testing - Brian Lowe*
3. *Test and Design for Testability in Mixed Signal ICs - Jose L Huertas*
4. *High Speed* Analog Design and Application Seminar - Texas Instruments.
5. *Recent literature in Testability of Analog / Mixed-Signal Circuits & High Speed Circuit Design.*

Course outcomes

At the end of the course student will be able

Course Code	**:**	**EC679**
Course Title	**:**	**High Speed System Design**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

Course Content

Functions of an Electronic Package, Packaging Hierarchy, IC packaging requirements and properties; materials and substrates; Interconnect Capacitance, Resistance and Inductance fundamentals;; IC assembly: , Wire bonding, Tape Automated Bonding, Flip Chip, wafer-level packaging; impact on reliability and testability

Overview of Transmission line theory, Clock Distribution, Noise Sources, power Distribution, signal distribution, EMI; crosstalk and nonideal effects; signal integrity: impact of packages, vias, traces, connectors; non-ideal return current paths, high frequency power delivery, simultaneous switching noise; system-level timing analysis and budgeting; methodologies for design of high speed buses; radiated emissions and minimizing system noise;

Practical aspects of measurement at high frequencies; high speed oscilloscopes and logic analyzers

Printed Circuit Board: Anatomy, CAD tools for PCB design, Standard fabrication, Microvia Boards. Board Assembly: Surface Mount Technology, Through Hole Technology, Process Control and Design challenges. Thermal Management, Heat transfer fundamentals, Thermal conductivity and resistance, Conduction, convection and radiation cooling requirements.

Reliability, Basic concepts, Environmental interactions. Thermal mismatch and fatigue failures thermo mechanically induced electrically induced chemically induced. Electrical Testing: System level electrical testing, Interconnection tests, Active Circuit Testing, Design for Testability.

Text Books

1. *Howard Johnson , Martin Graham, High Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 1993*

Reference Books

1. *High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices", Stephen H. Hall, Garrett W. Hall, James A. McCall, August 2000, Wiley-*

IEEE Press

2. *Tummala, Rao R., Fundamentals of Microsystems Packaging, McGraw Hill, 2001*
3. *William J. Dally , John W. Poulton , Digital Systems Engineering, Cambridge University Press, 2008)*
4. *R.G. Kaduskar and V.B.Baru, Electronic Product design, Wiley India, 2011.*
5. *Recent literature in High Speed System Design.*

Course outcomes

At the end of the course student will be able

Course Code	**:**	**EC612**
Course Title	**:**	**DSP Architecture**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objective

- To give an exposure to the various fixed point and floating point DSP architectures and to implement real time applications using these processors.

Course Content

Fixed-point DSP architectures. TMS320C54X, ADSP21XX, DSP56XX architecture details. Addressing modes. Control and repeat operations. Interrupts. Pipeline operation. Memory Map and Buses. TMS320C55X architecture and its comparison.

Floating-point DSP architectures. TMS320C67X, DSP96XX architectures. Cache architecture. Floating-point Data formats. On-chip peripherals. Memory Map and Buses.

On-chip peripherals and interfacing. Clock generator with PLL. Serial port. McBSP. Parallel port. DMA. EMIF. Serial interface- Audio codec. Sensors. A/D and D/A interfaces. Parallel interface- RAM and FPGA. RF transceiver interface.

DSP tools and applications. Implementation of Filters, DFT, QPSK Modem, Speech processing. Video processing, Video Encoding / Decoding. Biometrics. Machine Vision. High performance computing (HPC).

Digital Media Processors. Video processing sub systems. Multi-core DSPs. OMAP. CORTEX, SHARC, SIMD, MIMD Architectures.

Text Books

1. *B.Venkataramani&M.Bhaskar," Digital Signal Processor, Architecture, Programming and Applications",(2/e), McGraw- Hill,2010*
2. *S.Srinivasan&Avtar Singh, "Digital Signal Processing, Implementations using DSP Microprocessors with Examples from TMS320C54X", Brooks/Cole, 2004*

Reference Books

1. *S.M.Kuo&Woon-Seng S.Gan, "Digital Signal Processors: Architectures, Implementations, and Applications", Printice Hall, 2004.*
2. *N. Kehtarnavaz& M. Kerama, "DSP System Design using the TMS320C6000", Printice Hall, 2001.*
3. *S.M. Kuo&B.H.Lee,"Real-Time Digital Signal Processing, Implementations, Applications and Experiments with the TMS320C55X", John Wiley, 2001.*
4. *Recent literature in DSP Architecture.*

Course outcomes

At the end of the course student will be able

CO1: learn the architecture details fixed and floating point DSPs

CO2: infer about the control instructions, interrupts, and pipeline operations, memory and buses.

CO3: illustrate the features of on-chip peripheral devices and its interfacing with real time application devices.

CO4: learn to implement the signal processing algorithms and applications in DSPs.

CO5: learn the architecture of advanced DSPs.

Course Code	**:**	**EC613**
Course Title	**:**	**High Speed Communication Networks**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To impart the students a thorough exposure to the various high speed networking technologies and to analyse the methods adopted for performance modeling , traffic management and routing

Course Content

The need for a protocol architecture, The TCP/IP protocol architecture, Internetworking, Packet switching networks, Frame relay networks, Asynchronous Transfer mode (ATM) protocol architecture, High speed LANs. Multistage networks

Overview of probability and stochastic process, Queuing analysis, single server and multi-server queues, queues with priorities, networks of queues, Self similar Data traffic

Congestion control in data networks and internets, Link level flow and error control, TCP traffic control, Traffic and congestion control in ATM networks

Overview of Graph theory and least cost paths, Interior routing protocols, Exterior routing protocols and multicast.

Quality of service in IP networks, Integrated and differentiated services, Protocols for QOS support-Resource reservation protocol, Multiprotocol label switching, Real time transport protocol.

Text Books

1. *W. Stallings," High Speed networks and Internets", second edition, Pearson Education,2002*
2. *A. Pattavina,"Switching Theory", Wiley, 1998.*
3. *J. F. Kurose and K. W. Ross", Computer networking" 3rd edition, Pearson education,2005*

Reference Books

1. *Mischa Schwartz," Telecommunication networks, protocols, modeling and analysis", Pearson education,2004*
2. *Giroux, N. and Ganti, S." Quality of service in ATM networks", Prentice Hall ,1999*
3. *Recent literature in High Speed Communication Networks.*

Course outcomes

At the end of the course student will be able

Students are able to

CO1: compare and analyse the fundamental principles of various high speed communication networks and their protocol architectures

CO 2: analyse the methods adopted for performance modeling of traffic flow and estimation

CO 3: examine the congestion control issues and traffic management in TCP/IP and ATM networks

CO 4: compare, analyse and implement the various routing protocols in simulation software tools

CO 5: examine the various services.

Course Code	:	**EC615**
Course Title	:	**Digital Image Processing**
Number of Credits	:	**3**
Course Type	:	**Elective**

Course Learning Objective

- To explore various techniques involved in Digital Image Processing.

Course Content

Elements of Visual perception. Image sensing and Acquisition. Imaging in different bands. Digital Image Representation. Relationship between pixels. Image transformations: 2D-DFT, DCT, DST, Hadamard, Walsh, Hotelling transformation, 2D-Wavelet transformation, Wavelet packets.

Image Enhancements in spatial domain and Frequency domain. Image Restoration techniques. Color Image processing.

Error free compression: Variable length coding, LZW, Bit-plane coding, Lossless predictive coding Lossy compression: Lossy predictive coding, transform coding, wavelet coding. Image compression standards (CCITT, JPEG, JPEG 2000) and Video compression standards.

Summary of morphological operations in Binary and Gray Images. Image segmentation: Point, Line and Edge segmentation. Edge linking and Boundary detection. Segmentation using thresholding, Region based segmentation. Segmentation by morphological watersheds. Use of motion in segmentation.

Feature Extraction from the Image: Boundary descriptors, Regional descriptors, Relational descriptors. Dimensionality reduction techniques, Discriminative approach and the Probabilistic approach for image pattern recognition.

Text Books

1. *R. C.Gonzalez, R.E.Woods," Digital Image processing", Pearson edition, Inc3/e, 2008.*
2. *A.K.Jain," Fundamentals of Digital Image Processing", PHI,1995*

Reference Books

1. *J.C. Russ," The Image Processing Handbook", (5/e), CRC, 2006*
2. *R.C.Gonzalez & R.E. Woods; "Digital Image Processing with MATLAB", Prentice Hall, 2003*
3. *E.S.Gopi, "Digital Image processing using Matlab", Scitech publications, 2005*
4. *Recent literature in Digital Image Processing***.**

Course outcomes

At the end of the course student will be able

CO1: understand the need for image transforms different types of image transforms and their properties.

CO2: develop any image processing application.

CO3: understand the rapid advances in Machine vision.

CO4: learn different techniques employed for the enhancement of images.

CO5: learn different causes for image degradation and overview of image restoration techniques.

CO6: understand the need for image compression and to learn the spatial and frequency domain techniques of image compression.
CO7: learn different feature extraction techniques for image analysis and recognition.

Course Code	**:**	**EC616**
Course Title	**:**	**RF MEMS**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objective

- To impart knowledge on basics of MEMS and their applications in RF circuit design.

Course Content

Micromachining Processes - methods, RF MEMS relays and switches. Switch parameters. Actuation mechanisms. Bistable relays and micro actuators. Dynamics of switching operation.

MEMS inductors and capacitors. Micro-machined inductor. Effect of inductor layout. Modeling and design issues of planar inductor. Gap-tuning and area-tuning capacitors. Dielectric tunable capacitors.

MEMS phase shifters. Types. Limitations. Switched delay lines. Fundamentals of RF MEMS Filters.

Micro-machined transmission lines. Coplanar lines. Micro-machined directional coupler and mixer.

Micro-machined antennas. Microstrip antennas – design parameters. Micromachining to improve performance. Reconfigurable antennas.

Text Books

1. *Vijay. K. Varadan, K.J. Vinoy, and K.A. Jose, "RF MEMS and their Applications", Wiley-India, 2011.*

Reference Books

1. *H. J. D. Santos, "RF MEMS Circuit Design for Wireless Communications", Artech House, 2002.*
2. *G. M. Rebeiz, "RF MEMS Theory, Design, and Technology", Wiley, 2003.*
3. *Recent literature in RF MEMS.*

Course outcomes

At the end of the course student will be able

CO1: learn the Micromachining Processes

CO2: learn the design and applications of RF MEMS inductors and capacitors.

CO3: learn about RF MEMS Filters and RF MEMS Phase Shifters.

CO4: learn about the suitability of micro-machined transmission lines for RF MEMS

CO5: learn about the Micro-machined Antennas and Reconfigurable Antennas.

Course Code	**:**	**EC626**
Course Title	**:**	**Bio MEMS**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objective

- To train the students in the design aspects of Bio MEMS devices and Systems. To make the students aware of applications in various medical specialists especially the Comparison of conventions methods and Bio MEMS usage.

Course Content

Introduction-The driving force behind Biomedical Applications – Biocompatibility - Reliability Considerations-Regularity Considerations – Organizations - Education of Bio MEMS-Silicon Micro fabrication-Soft Fabrication techniques

Micro fluidic Principles- Introduction-Transport Processes- Electro kinetic Phenomena-Micro valves –Micro mixers- Micro pumps.

SENSOR PRINCIPLES and MICRO SENSORS: Introduction-Fabrication-Basic Sensors-Optical fibers-Piezo electricity and SAW devices-Electrochemical detection-Applications in Medicine

MICRO ACTUATORS and DRUG DELIVERY: Introduction-Activation Methods-Micro actuators for Micro fluidics-equivalent circuit representation-Drug Delivery

MICRO TOTAL ANALYSIS: Lab on Chip-Capillary Electrophoresis Arrays-cell, molecule and Particle Handling-Surface Modification-Microsphere-Cell based Bioassay Systems

Detection and Measurement Methods-Emerging Bio MEMS Technology-Packaging, Power, Data and RF Safety-Biocompatibility, Standards

Text Book

1. *Steven S. Saliterman, Fundamentals of Bio MEMS and Medical Micro devices, Wiley Interscience, 2006.*

Reference Books

1. *Albert Folch , Introduction to Bio MEMS, CRC Press, 2012*
2. *Gerald A. Urban, Bio MEMS, Springer, 2006*
3. *Wanjun wang, steven A. Soper, Bio MEMS, 2006.*
4. *M. J. Madou, "Fundametal of Micro fabrication",* 2002.
5. *G.T. A. Kovacs, "Micro machined Transducers Sourcebook", 1998*.
6. *Recent literature in Bio MEMS.*

Course outcomes

At the end of the course student will be able

CO1: learn and realize the MEMS applications in Bio Medical Engineering

CO2: understand the Micro fluidic Principles and study its applications.

CO3: learn the applications of Sensors in Health Engineering.

CO4: learn the principles of Micro Actuators and Drug Delivery system

CO5: learn the principles and applications of Micro Total Analysis