M. Tech.

IN

VLSI SYSTEM

CURRICULUM

(For students admitted in 2019-2021)
Institute Vision and Mission

Vision
- To be a university globally trusted for technical excellence where learning and research integrate to sustain society and industry.

Mission
- To offer undergraduate, postgraduate, doctoral and modular programmes in multi-disciplinary / inter-disciplinary and emerging areas.
- To create a converging learning environment to serve a dynamically evolving society.
- To promote innovation for sustainable solutions by forging global collaborations with academia and industry in cutting-edge research.
- To be an intellectual ecosystem where human capabilities can develop holistically.

Department Vision and Mission

Vision
- To excel in education and research in Electronics and Communication Engineering

Mission
- To educate with the state of art technologies to meet the growing challenges of the industry.
- To carry out research through constant interaction with research organizations and industry.
- To equip the students with strong foundations to enable them for continuing Education.

Program Educational Objectives (PEOs)

- **PEO1**: Graduates will be successful in facing the challenges in their professional career in industry, government and academia by integrating the existing and advanced knowledge in VLSI Systems to solve complex problems in Electronics and Communication engineering.

- **PEO2**: Graduates will be efficient in adapting new technologies, achieve excellence in their professional career, lead research as well as development projects/activities and establish themselves as successful professional.

- **PEO3**: Graduates will practice and inspire high ethical and technical standards, possess technical competency in VLSI Systems and take up higher studies.
Program Outcomes (POs)

- **PO1**: To acquire in-depth knowledge in Embedded System, Digital VLSI and Mixed Signal Systems including wider and global perspective, with an ability to discriminate, evaluate, analyse and synthesise existing and new knowledge, and integration of the same for enhancement of knowledge.

- **PO2**: To design and analyse complex VLSI/Embedded circuits critically, using appropriate analytical methods as well as front end and back end tools including prediction and modelling at industry standards with an understanding of the limitations.

- **PO3**: An ability to independently carry out research /investigation and development work to solve practical problems and have the preparedness for lifelong learning.

- **PO4**: To comprehend and write effective reports and design documentation by adhering to appropriate standards, make effective presentations, and give and receive clear instructions.

- **PO5**: Students should be able to demonstrate a degree of mastery in VLSI/Embedded system by way of developing new algorithms, techniques, solutions to domestic and industrial problems.

- **PO6**: To acquire professional code of conduct, ethics of research and scholarship, consideration of the impact of research outcomes on professional practices and an understanding of responsibility to contribute to the community for sustainable development of society.
CURRICULUM

The total minimum credits for completing the M.Tech. Programme in VLSI System is 66.

SEMESTER I

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>1.</td>
<td>MA617</td>
<td>Graph Theory and Discrete Optimization</td>
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<td>EC651</td>
<td>Analog VLSI</td>
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<td>Basics of VLSI</td>
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<td>7.</td>
<td>EC655</td>
<td>HDL Programming Laboratory</td>
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SEMESTER II

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<td>VLSI System Testing</td>
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<td>EC654</td>
<td>Electronic Design Automation Tools</td>
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<td>3.</td>
<td>EC656</td>
<td>Design of ASICs</td>
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<td>Elective V</td>
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<td>Elective VI</td>
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<td>EC658</td>
<td>Analog IC Design Laboratory</td>
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<td>EC660</td>
<td>ASIC – CAD Laboratory</td>
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### SEMESTER IV

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<td>PROJECT WORK - PHASE II</td>
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### LIST OF ELECTIVES

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<tr>
<td>1.</td>
<td>EC661</td>
<td>Digital System Design</td>
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<td>2.</td>
<td>EC662</td>
<td>Modelling and Synthesis with Verilog HDL</td>
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<td>EC663</td>
<td>Optimization of Digital Signal Processing structures for VLSI</td>
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<td>EC664</td>
<td>Cognitive Radio</td>
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<td>EC665</td>
<td>VLSI Process Technology</td>
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<td>EC666</td>
<td>Analysis and Design of Digital Systems using VHDL</td>
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<td>EC667</td>
<td>Advanced Computer Architecture</td>
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<td>EC668</td>
<td>Low Power VLSI Systems</td>
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<td>EC669</td>
<td>VLSI Digital Signal Processing Systems</td>
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<td>EC670</td>
<td>Asynchronous System Design</td>
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<td>EC671</td>
<td>Advanced Digital Design</td>
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<td>Physical Design Automation</td>
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<td>EC673</td>
<td>Mixed - Signal Circuit Design</td>
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<td>EC674</td>
<td>RF circuits</td>
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<td>EC675</td>
<td>Functional Verification using Hardware Verification Languages</td>
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<td>16.</td>
<td>EC676</td>
<td>Testability of Analog / Mixed-Signal Circuits and High Speed Circuit Design</td>
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<td>17.</td>
<td>EC677</td>
<td>High Speed System Design</td>
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<td>18.</td>
<td>EC678</td>
<td>Modelling of Solid-State Devices</td>
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<td>EC679</td>
<td>Nano-Scale Devices: Modelling and Circuits</td>
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<td>EC680</td>
<td>Embedded System Design</td>
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<td>EC681</td>
<td>Internet of Things</td>
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<td>EC682</td>
<td>Design and Testing of Advanced Semiconductor Memories</td>
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<td>23.</td>
<td>EC683</td>
<td>FPGA Based System Design</td>
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<td>EC684</td>
<td>Bio-Medical CMOS ICs</td>
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<td>EC685</td>
<td>On-chip Antenna Design</td>
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<td>EC612</td>
<td>DSP Architecture</td>
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<td>EC613</td>
<td>High Speed Communication Networks</td>
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<td>28.</td>
<td>EC615</td>
<td>Digital Image Processing</td>
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<td>EC616</td>
<td>RF MEMS</td>
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<td>30.</td>
<td>EC626</td>
<td>Bio MEMS</td>
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LIST OF OPEN ELECTIVES

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<td>4.</td>
<td>EC668</td>
<td>Low Power VLSI Systems</td>
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</table>
Course Learning Objective

- To have general awareness of some application oriented concepts in discrete structures and apply them as a tool in the problems related to general communication network.

Course Content

Basic definitions, examples and some results, relating degree, walk, trail, path, tour, cycle, complement of a graph, self-complementary graph, Connectedness, Connectivity, distance, shortest path, radius, diameter and Bipartite graphs. Some eccentric properties of graphs, tree, spanning tree, coding of spanning tree. Number of spanning trees in a complete graph. Recursive procedure to find number of spanning trees. Construction of spanning trees.


Chromatic number; vertex chromatic number of a graph, edge chromatic number of a graph (only properties and examples)-application to colouring. Planar graphs, Euler’s formula, maximum number of edges in a planar graph, some problems related to planarity and non-planarity. Five colour theorem, Vertex Covering, Edge Covering, Vertex independence number, Edge independence number, relation between them and number of vertices of a graph.

Matching theory, maximal matching and algorithms for maximal matching. Perfect matching (only properties and applications to regular graphs). Tournaments, some simple properties and theorems on strongly connected tournaments. Application of Eulerian digraphs.

DFS-BFS algorithm, shortest path algorithm, Min-spanning tree and Max-spanning tree algorithm, Planarity algorithm. Flows in graphs; Maxflow mincut theorem, algorithm for maxflow. PERT-CPM. Complexity of algorithms; P-NP-NPC-NP hard problems and examples.

Text Books


Reference Books


Course outcomes

At the end of the course student will be able to

- CO1: understand the various types of graphs, graph properties and give examples for the given property
- CO2: model the given problem from their field to underlying graph model.
- CO3: proceed to solve the problem either through approximation algorithm or exact algorithm depending on the problem nature.
- CO4: appreciate the applications of digraphs and graphs in various communication networks.
- CO5: appreciate the applications of graphs and digraphs in various other fields.
Course Learning Objectives

- To develop the ability to design and analyze MOS based Analog VLSI circuits to draw the equivalent circuits of MOS based Analog VLSI and analyze their performance.
- To develop the skills to design analog VLSI circuits for a given specification.

Course Content

Basic MOS Device Physics – General Considerations, MOS I/V Characteristics, Second Order effects, MOS Device models. Short Channel Effects and Device Models. Single Stage Amplifiers – Basic Concepts, Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage.


Bandgap References, Introduction to Switched Capacitor Circuits, Nonlinearity and Mismatch.

Text Books


Reference Books

4. Recent literature in Analog IC Design.

Course outcomes

At the end of the course student will be able to

CO1: draw the equivalent circuits of MOS based Analog VLSI and analyse their performance.
CO2: design analog VLSI circuits for a given specification.
CO3: analyse the frequency response of the different configurations of an amplifier.
CO4: understand the feedback topologies involved in the amplifier design.
CO5: appreciate the design features of the differential amplifiers.
Course Code : EC653
Course Title : Basics of VLSI
Number of Credits : 3
Course Type : Core

Course Learning Objectives

- To provide rigorous foundation in MOS and CMOS digital circuits
- To train the students in transistor budgets, clock speeds and the growing challenges of power consumption and productivity

Course Content

Introduction to CMOS circuits: MOS transistors, CMOS combinational logic gates, multiplexers, latches and flip-flops, CMOS fabrication and layout, VLSI design flow.

MOS transistor theory: Ideal I-V and C-V characteristics, non-ideal I-V effects, DC transfer characteristics, Switch level RC delay models.

CMOS technologies: Layout design rules, CMOS process enhancement, Technology related CAD issues.

Circuit characterization and performance estimation: Delay estimation, Logical effort and transistor sizing, Power dissipation, Interconnect design margin, Reliability, Scaling.

Combinational circuit design: Static CMOS, Ratioed circuits, Cascode voltage switch logic, Dynamic circuits, Pass transistor circuits.

Text Books


Reference Books

2. Recent literature in Basics of VLSI.

Course outcomes

At the end of the course student will be able to
CO1: implement the logic circuits using MOS and CMOS technology.
CO2: analyse various circuit configurations and their applications
CO3: analyse the merits of circuits according to the technology and applications change.
CO4: design low power CMOS VLSI circuits.
CO5: understand the rapid advances in CMOS Technology
<table>
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<tr>
<th>Course Code</th>
<th>EC655</th>
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<tr>
<td>Course Title</td>
<td>HDL Programming Laboratory</td>
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<td>Course Type</td>
<td>Laboratory</td>
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**List of Experiments**

1. Adder/ Subtractor
2. Multiplexer/ Demultiplexer
3. Encoder/ Priority Encoder
4. Code Converter
5. Flip flop
6. Shift Register/ Universal Shift Register
7. Comparator
8. Up counter/ Down counter
9. Udps
10. Memory – ROM, RAM
11. Array Multiplier/ Array Multiplier With Pipelining
12. Fir Filter/ Fir Filter With Pipelining

**List of Experiments**

1. Design of 8-bit Carry Skip Adder and Carry Save Adder
2. Design of 4-bit Array Multiplier with and without Pipelining
3. Design of 4-tap FIR Filter with and without Pipelining
4. Design of FIFO
5. Design of Sequence Detector
6. Design of 8-bit ALU
7. Project: Design of 16-point FFT

**Course outcomes:**
After successful completion of the laboratory course, the students are able to

CO1: to learn the basic HDL functions
CO2: Design and analyse the combinational and sequential circuits using Verilog HDL tools.
CO3: Perform FPGA Implementation for Verilog HDL designs on development board
CO4: Implement FIR algorithms in FPGA
CO5: Implement FFT algorithm in FPGA
**Course Code**: EC652  
**Course Title**: VLSI System Testing  
**Number of Credits**: 3  
**Course Type**: Core

**Course Learning Objective**  
- To expose the students, the basics of testing techniques for VLSI circuits and Test Economics.

**Course Content**  

Universal test sets: Pseudo-exhaustive and iterative logic array testing. Clocking schemes for delay fault testing. Testability classifications for path delay faults. Test generation and fault simulation for path and gate delay faults.


Design for testability: Scan design, Partial scan, use of scan chains, boundary scan, DFT for other test objectives, Memory Testing.

Built-in self-test: Pattern Generators, Estimation of test length, Test points to improve testability, Analysis of aliasing in linear compression, BIST methodologies, BIST for delay fault testing.

**Text Books**  

**Reference Books**  
4. Recent literature in VLSI System Testing.

**Course outcomes**  
At the end of the course student will be able to  
CO1: apply the concepts in testing which can help them design a better yield in IC design.  
CO2: tackle the problems associated with testing of semiconductor circuits at earlier design levels so as to significantly reduce the testing costs.  
CO3: analyse the various test generation methods for static and dynamic CMOS circuits.  
CO4: identify the design for testability methods for combinational and sequential CMOS circuits.  
CO5: recognize the BIST techniques for improving testability.
Course Code : EC654
Course Title : Electronic Design Automation Tools
Number of Credits : 3
Course Type : Core

Course Learning Objective
- To make the students exposed to Front end and Back end VLSI CAD tools.

Course Content
OS Architecture: System settings and configuration. Introduction to UNIX commands handling directories, Filters and Piping, Wildcards and Regular expression, Power Filters and Files Redirection. Working on Vi editor, Basic Shell Programming, TCL Scripting language.


System Verilog- Introduction, Design hierarchy, Data types, Operators and language constructs. Functional coverage, Assertions, Interfaces and test bench structures.

Text Books

Reference Books

Course outcomes
After successful completion of the course the students are able to
CO1: execute the special features of VLSI back end and front end CAD tools and UNIX shell script
CO2: write Pspice code for any electronics circuit and to perform monte-carlo analysis and sensitivity/worst case analysis.
CO3: design synthesizable Verilog and VHDL code.
CO4: explain the difference between Verilog and system Verilog and are able to write system Verilog code.
CO5: Model Analog and Mixed signal blocks using Verilog A and Verilog AMS.
Course Learning Objectives

- To prepare the student to be an entry-level industrial standard ASIC or FPGA designer.
- To give the student an understanding of issues and tools related to ASIC/FPGA design and implementation.
- To give the student an understanding of basics of System on Chip and Platform based design.
- To give the student an understanding of High performance algorithms.

Course Content

Introduction to Technology, Types of ASICs, VLSI Design flow, Design and Layout Rules, Programmable ASICs – Anti-fuse, SRAM, EPROM, EEPROM based ASICs. Programmable ASIC logic cells and I/O cells. Programmable interconnects. Advanced FGPs and CPLDs and Soft-core processors. Self-Study: Multi-core processors, High performance computing (HPC), Cache, High speed memories (DDR4), High speed serdes (56Gbps, PAM4), GPU, High performance algorithms for ASICs/ SoCs, FSM design, clock domain crossing, FIFOs. Core (ARM) and IOs.


Semicustom Approach: Synthesis (RTL to GATE netlist) - Introduction to Constraints (SDC), Introduction to Static Timing Analysis (STA). Place and Route (Logical to Physical Implementation): Floorplan and Power-Plan, Placement, Clock Tree Synthesis (clock planning), Routing, Timing Optimization, GDS generation.


System-On-Chip Design - SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures. Case study: FSM design, clock domain crossing, FIFOs. Core (ARM) and IOs(I2C, PWM, GPIO, SPI, NAND, Ethernet, USB, high speed serdes etc. are interconnected through AXI/APB buses (protocols and interconnects)

Text Books


Reference Books

6. Recent literature in Design of ASICs.

Course outcomes
At the end of the course student will be able to
CO1: explain VLSI tool-flow and appreciate FPGA architecture.
CO2: describe the issues involved in ASIC design, including technology choice, design management, tool-flow, verification, debug and test, as well as the impact of technology scaling on ASIC design.
CO3: explain the algorithms used for ASIC construction
CO4: analyse the basics of System on Chip, On chip communication architectures like AMBA, AXI and utilizing Platform based design.
CO5: synthesize high performance algorithms available for ASICs
Course Code : EC658
Course Title : Analog IC Design Laboratory
Number of Credits : 2
Course Type : Laboratory

List of Experiments
1. Characteristics of NMOS and PMOS Transistor
2. Design of Common Source Amplifier with different Loads
3. Design of Common Gate Amplifier
4. Design of Common Drain Amplifier
5. Design of Single stage Cascode Amplifiers
6. Design of Current Mirrors
7. Design of Differential Amplifiers with Different Loads
8. Design of Two stage Opamp
9. Design of Telescopic Cascode Opamp
10. Design of Folded Cascode Opamp

Course outcomes

After successful completion of the laboratory course, the students are able to
CO1: Introduce industry standard Analog IC design EDA tool
CO2: Practical learning and understanding of Analog amplifiers, current mirrors etc.
CO3: Solve analog design problems by changing the design parameter of the circuit with the help
   of Cadence Virtuoso.
CO4: understand the working of circuits and enhance the analog design skills.
CO5: Learn the art of analog layout in IC design.
Course Code : EC 660
Course Title : ASIC – CAD Laboratory
Number of Credits : 2
Course Type : Laboratory

List of Experiments
1. Adder/ Subtractor
2. Multiplexer/ Demultiplexer
3. 8-bit Counter
4. Signed Pipelined Multiplier
5. Accumulator
6. MAC
7. Memory

The above experiments are carried out using the following tools:
1. Model SIM
2. Cadence
3. Synopsis
4. Mentor Graphics
5. Xilinx Plan ahead

List of Experiments
1. Design of MOD 10 Counter using Verilog
2. Design of MAC Unit using Verilog
3. Design of 8 bit Signed Booth Multiplier using Verilog
4. Design of 4 tap FIR Filter using Verilog
5. Design of Address Generator block for WiMAX Interleaver using Verilog
6. Project: Design of Vending Machine Block using Verilog

The above experiments are carried out using the following tools:
1. Xilinx ISE Design Suite
2. Cadence
3. Synopsis

Course outcomes:
After successful completion of the laboratory course, the students are
CO1: Familiar with sophisticated VLSI CAD tools available in the lab.
CO2: Able to design and implement any ASIC designs using the latest VLSI CAD tools.
CO3: Perform full custom ASIC design of digital blocks
CO4: Learn advanced features in physical design
CO5: Complete cycle from design to chip tape-out procedure
Course Code : EC661
Course Title : Digital System Design
Number of Credits : 3
Course Type : Elective

Course Learning Objective
- To get an idea about designing complex, high speed digital systems and how to implement such design.

Course Content
Mapping algorithms into Architectures: Data path synthesis, control structures, critical path and worst case timing analysis. FSM and Hazards.


Data path and array subsystems: Addition / Subtraction, Comparators, counters, coding, multiplication and division. SRAM, DRAM, ROM, serial access memory, context addressable memory.

Reconfigurable Computing- Fine grain and Coarse grain architectures, Configuration architectures- Single context, Multi context, partially reconfigurable, Pipeline reconfigurable, Block Configurable, Parallel processing.

Text Books

Reference Books
6. Recent literature in Digital System Design.

Course outcomes
At the end of the course student will be able to
CO1: identify mapping algorithms into architectures.
CO2: summarize various delays in combinational circuit and its optimization methods.
CO3: summarize circuit design of latches and flip-flops.
CO4: construct combinational and sequential circuits of medium complexity that is based on VLSIs, and programmable logic devices.
CO5: summarize the advanced topics such as reconfigurable computing, partially reconfigurable, Pipeline reconfigurable architectures and block configurable.
Course Code : EC662
Course Title : Modeling and Synthesis with Verilog HDL
Number of Credits : 3
Course Type : Elective

Course Learning Objectives
- To design combinational, sequential circuits using Verilog HDL.
- To understand behavioural and RTL modelling of digital circuits
- To verify that a design meets its timing constraints, both manually and through the use of computer aided design tools
- To simulate, synthesize, and program their designs on a development board
- To verify and design the digital circuit by means of Computer Aided Engineering tools which involves in programming with the help of Verilog HDL.

Course Content
Hardware modelling with the verilog HDL. Encapsulation, modelling primitives, different types of description.
Logic system, data types and operators for modelling in verilog HDL. Verilog Models of propagation delay and net delay path delays and simulation, inertial delay effects and pulse rejection.
Behavioural descriptions in verilog HDL. Synthesis of combinational logic.

HDL-based synthesis - technology-independent design, styles for synthesis of combinational and sequential logic, synthesis of finite state machines, synthesis of gated clocks, design partitions and hierarchical structures.

Synthesis of language constructs, nets, register variables, expressions and operators, assignments and compiler directives. Switch-level models in verilog. Design examples in verilog.

Text Books

Reference Books
3. Recent literature in Modeling and Synthesis with Verilog HDL.

Course outcomes
At the end of the course student will be able to
CO1: understand the basic concepts of verilog HDL
CO2: model digital systems in verilog HDL at different levels of abstraction
CO3: know the simulation techniques and test bench creation.
CO4: understand the design flow from simulation to synthesizable version
CO5: get an idea of the process of synthesis and post-synthesis
Course Code : EC663
Course Title : Optimizations of Digital Signal Processing Structures for VLSI
Number of Credits : 3
Course Type : Elective

Course Learning Objectives
- To understand the various VLSI architectures for digital signal processing.
- To know the techniques of critical path and algorithmic strength reduction in the filter structures.
- To enable students to design VLSI system with high speed and low power.
- To encourage students to develop a working knowledge of the central ideas of implementation of DSP algorithm with optimized hardware.

Course Content
An overview of DSP concepts, Pipelining of FIR filters. Parallel processing of FIR filters. Pipelining and parallel processing for low power, Combining Pipelining and Parallel Processing.


Algorithms for fast convolution: Cook-Toom Algorithm, Cyclic Convolution. Algorithmic strength reduction in filters and transforms: Parallel FIR Filters, DCT and inverse DCT, Parallel Architectures for Rank-Order Filters.

Synchronous pipelining and clocking styles, clock skew and clock distribution in bit level pipelined VLSI designs. Wave pipelining, constraint space diagram and degree of wave pipelining. Implementation of wave-pipelined systems, Asynchronous pipelining.

Text Book

Reference Books
7. Recent literature in Optimizations of Digital Signal Processing Structures for VLSI.

Course outcomes
At the end of the course student will be able to
CO1: understand the overview of DSP concepts and design architectures for DSP algorithms.
CO2: improve the overall performance of DSP system through various transformation and optimization techniques.
CO3: perform pipelining and parallel processing on FIR and IIR systems to achieve high speed and low power.
CO4: optimize design in terms of computation complexity and speed.
CO5: understand clock based issues and design asynchronous and wave pipelined systems.
Course Code : EC664
Course Title : Cognitive Radio
Number of Credits : 3
Course Type : Elective

Course Learning Objective
- This subject introduces the fundamentals of multi rate signal processing and cognitive radio.

Course Content


Text Books

Reference Books
7. Recent literature in Cognitive Radio.

Course outcomes
At the end of the course student will be able to
CO1: gain knowledge on multirate systems.
CO2: develop the ability to analyze, design, and implement any application using FPGA.
CO3: be aware of how signal processing concepts can be used for efficient FPGA based system design.
CO4: understand the rapid advances in Cognitive radio technologies.
CO5: explore DDFS, CORDIC and its application.
Course Learning Objective

- To provide rigorous foundation in MOS and CMOS fabrication process.

Course Content


Optical, electron, X-ray and ion lithography methods. Plasma properties, size, control, etch mechanism, etch techniques and equipments.


Ion implantation and metallization. Process simulation of ion implementation, diffusion, oxidation, epitaxy, lithography, etching and deposition. NMOS, CMOS, MOS memory and bipolar IC technologies. IC fabrication.

Analytical and assembly techniques. Packaging of VLSI devices.

Text Books


Reference Books


Course outcomes

At the end of the course student will be able to

CO1: appreciate the various techniques involved in the VLSI fabrication process.
CO2: understand the different lithography methods and etching process.
CO3: appreciate the deposition and diffusion mechanisms.
CO4: analyze the fabrication of NMOS, CMOS memory and bipolar devices
CO5: understand the nuances of assembly and packaging of VLSI devices.
Course Learning Objectives

- To prepare the student to understand the VHDL language feature to realize the complex digital systems.
- To design and simulate sequential and concurrent techniques in VHDL.
- To explain modeling of digital systems using VHDL and design methodology.
- To explain predefined attributes and configurations of VHDL.
- To understand behavioral, non-synthesizable VHDL and its role in modern design.

Course Content

An overview of design procedures for system design using CAD tools. Design verification tools. Examples using commercial PC based VLSI CAD tools. Design methodology based on VHDL. Basic concepts and structural descriptions in VHDL.

Characterizing hardware languages, objects and classes, signal assignments, concurrent and sequential assignments. Structural specification of hardware.

Design organization, parameterization and high level utilities, definition and usage of subprograms, packaging parts and utilities, design parameterization, design configuration, design libraries. Utilities for high-level descriptions.

Data flow and behavioural description in VHDL- multiplexing and data selection, state machine description, open collector gates, three state bussing, general dataflow circuit, updating basic utilities. Behavioural description of hardware.

CPU modelling for discrete design- Parwan CPU, behavioural description, bussing structure, data flow, test bench, a more realistic Parwan. Interface design and modelling. VHDL as a modelling language.

Text Books


Reference Books

4. Recent literature in Analysis and Design of Digital Systems using VHDL.

Course outcomes

At the end of the course student will be able to

CO1: model, simulate, verify, and synthesize with hardware description languages.

CO2: understand and use major syntactic elements of VHDL - entities, architectures, processes, functions, common concurrent statements, and common sequential statements.

CO3: design digital logic circuits in different types of modelling.

CO4: demonstrate timing and resource usage associated with modelling approach.

CO5: use computer-aided design tools for design of complex digital logic circuits.
Course Code : EC667
Course Title : Advanced Computer Architecture
Number of Credits : 3
Course Type : Elective

Course Learning Objective
- To give an exposure on look ahead pipelining- parallelism, multiprocessor scheduling, multithreading and various memory organizations.

Course Content


Text Books

Reference Book
2. Recent literature in Advanced Computer Architecture.

Course outcomes
At the end of the course student will be able to
CO1: apply the basic knowledge of partitioning and scheduling in Multiprocessors.
CO2: analyze and design cache memory, virtual memory and shared memory organizations.
CO3: distinguish and analyze the design properties of Linear and Non - Linear processors.
CO4: analyze the principles of multithreading in hybrid Architectures.
CO5: write any parallel programming models for various architectures and Applications.
Course Code : EC668
Course Title : Low Power VLSI Systems
Number of Credits : 3
Course Type : Elective

Course Learning Objective
- To expose the students to the low voltage device modeling, low voltage, low power VLSI CMOS circuit and system design.

Course Content
Evolution of CMOS technology, CMOS fabrication process, shallow trench isolation, Lightly-doped drain, Buried channel. Bi-CMOS and SOI CMOS technologies, second order effects, Modeling of MOS devices, Threshold voltage, Body effect, Short channel and Narrow channel effects, Electron temperature, MOS capacitance.

CMOS inverters, Differential static logic circuits, Pass transistor, Bi-CMOS, SOI CMOS, Low voltage and low power CMOS static logic circuit design techniques.

Basic concepts of dynamic logic circuits. Charge sharing, Noise and race problems, NORA, Zipper, Domino, Dynamic differential, BiCMOS, low voltage and low power dynamic logic techniques.

CMOS memory circuits, SRAM, DRAM, Bi-CMOS and Nonvolatile memory circuits.

Basics of clock gating and power gating. Key characteristics of the Unified Power Format (UPF) in low power design. CMOS VLSI systems, Adder circuits, Multipliers and advanced structures – PLA, PLL, DLL and processing unit.

Text Books

Reference Books

Course outcomes
At the end of the course student will be able to
CO1: acquire the knowledge about various CMOS fabrication process and its modelling and infer about the second order effects of MOS transistor characteristics.
CO2: analyze and implement various CMOS low voltage and low power static logic circuits.
CO3: learn the design of various CMOS low voltage and low power dynamic logic circuits.
CO4: learn the different types of memory circuits and their design.
CO5: design and implementation of various structures for low power applications.
Course Code : EC669  
Course Title : VLSI Digital Signal Processing Systems  
Number of Credits : 3  
Course Type : Elective

Course Learning Objectives
- To enable students to design VLSI systems with high speed and low power.
- To encourage students to develop a working knowledge of the central ideas of implementation of DSP algorithm with optimized hardware.

Course Content


Bit level arithmetic Architectures- parallel multipliers, interleaved floor-plan and bit-plane-based digital filters, Bit serial multipliers, Bit serial filter design and implementation, Canonic signed digit arithmetic, Distributed arithmetic.

Redundant arithmetic - Redundant number representations, carry free radix-2 addition and subtraction, Hybrid radix-4 addition, Radix-2 hybrid redundant multiplication architectures, data format conversion, Redundant to Non-redundant converter.

Numerical Strength Reduction - Subexpression Elimination, Multiple Constant Multiplication, Subexpression Sharing in Digital Filters, Additive and Multiplicative Number Splitting.

Text Book

Reference Book

Course outcomes
At the end of the course student will be able to
CO1: explain various transforms and its corresponding architectures
CO2: describe the knowledge of effect of round off noise computation
CO3: design Bit level arithmetic Architectures and optimize the implementation of FIR filters and constant multipliers
CO4: design basic arithmetic units and realize their architecture for higher radices
CO5: create different numerical strength reduction techniques
Course Learning Objectives

- This subject introduces the fundamentals and performance of Asynchronous system
- To familiarize the dependency graphical analysis of signal transmission graphs
- To learn software languages and its syntax and operations for implementing Asynchronous Designs

Course Content

Fundamentals: Handshake protocols, Muller C-element, Muller pipeline, Circuit implementation styles, theory. Static data-flow structures: Pipelines and rings, Building blocks, examples


High-level languages and tools: Concurrency and message passing in CSP, Tangram program examples, Tangram syntax-directed compilation, Martin’s translation process, Using VHDL for Asynchronous Design. An Introduction to Balsa: Basic concepts, Tool set and design flow, Ancillary Balsa Tools


Text Books


Reference Books

4. Recent literature in Asynchronous System Design.

Course outcomes

At the end of the course student will be able to

CO1: understand the fundamentals of Asynchronous protocols
CO2: analyse the performance of Asynchronous System and implement handshake circuits
CO3: understand the various control circuits and Asynchronous system modules
CO4: gain the experience in using high level languages and tools for Asynchronous Design
CO5: learn commands and control flow of Balsa language for implementing Asynchronous Designs
Course Learning Objectives
- To make the students learn about graphical models and state diagram in designing optimized digital circuits.
- To provide the students a detailed knowledge of scheduling algorithm, synthesis of pipelined circuits and scheduling pipelined circuits
- To enable the students to design digital design with advanced technique like Sequential logic optimization and test the designed circuit Testability considerations.

Course Content

Scheduling algorithms-Scheduling with and without constraints. Scheduling algorithms for extended sequencing models. Scheduling pipelined circuits.


Text Books

Reference Books
5. Recent literature in Advanced Digital Design.

Course outcomes
At the end of the course student will be able to
CO1: understand advanced state of art techniques of digital design.
CO2: synthesis the circuits and evaluate its performance in terms of area, power and speed.
CO3: understand the use of scheduling algorithm.
CO4: gain in-depth knowledge of sequential digital circuits designed using resource sharing.
CO5: understand synchronization across clock domains, timing analysis, and Testability considerations.
Course Code : EC672
Course Title : Physical Design Automation
Number of Credits : 3
Course Type : Elective

Course Learning Objectives
- Understand the concepts of Physical Design Process such as partitioning, Floor planning, Placement and Routing.
- Discuss the concepts of design optimization algorithms and their application to physical design automation.
- Understand the concepts of simulation and synthesis in VLSI Design Automation
- Formulate CAD design problems using algorithmic methods

Course Content
VLSI design automation tools- algorithms and system design. Structural and logic design. Transistor level design. Layout design. Verification methods. Design management tools.


Floor planning and routing- floor planning concepts. Shape functions and floor planning sizing. Local routing. Area routing. Channel routing, global routing and its algorithms.

Simulation and logic synthesis- gate level and switch level modeling and simulation. Introduction to combinational logic synthesis. ROBDD principles, implementation, construction and manipulation. Two level logic synthesis.


Text Books

Reference Books
5. Recent literature in Physical Design Automation.

Course outcomes
At the end of the course student will be able to
CO1: Students are able to know how to place the blocks and how to partition the blocks while for designing the layout for IC.
CO2: Students are able to solve the performance issues in circuit layout.
CO3: Students are able to analyze physical design problems and Employ appropriate automation algorithms for partitioning, floor planning, placement and routing
CO4: Students are able to decompose large mapping problem into pieces, including logic optimization with partitioning, placement and routing
CO5: Students are able to analyze circuits using both analytical and CAD tools
Course Code: EC673
Course Title: Mixed - Signal Circuit Design
Number of Credits: 3
Course Type: Elective

Course Learning Objective
• To make the students to understand the design and performance measures concept of mixed signal circuit.

Course Content

Concepts of Mixed-Signal Design and Performance Measures. Introduction and Principle behind ADC’s and DAC’s - Performance Metrics of ADCs and DACs, Nyquist Rate DACs, Comparators-Characterization – Two stage comparators – open loop comparators, Nyquist rate ADCs: Flash, SAR, Pipelined, Time-interleaved ADCs. Overview of oversampling ADCs.

Design methodology for mixed signal IC design using gm/Id concept.


CMOS Digital Circuits Design: Design of MOSFET Switches and Switched-Capacitor Circuits, Layout Considerations.

Design of frequency and Q tunable continuous time filters.

Text Books

Course outcomes
At the end of the course student will be able to
CO1: appreciate the fundamentals of data converters and also optimized their performances.
CO2: understand the design methodology for mixed signal IC design using gm/Id concept.
CO3: analyze the design of current mirrors and operational amplifiers
CO4: design the CMOS digital circuits and implement its layout.
CO5: design the frequency and Q-tunable time domain filters.
Course Code : EC674
Course Title : RF Circuits
Number of Credits : 3
Course Type : Elective

Course Learning Objectives
- To impart knowledge on basics of CMOS IC design at RF frequencies.
- To be familiar with the circuits used in RF front end in transceiver design.

Course Content

High frequency amplifier design – Types of amplifiers: Narrowband and Wideband Amplifiers - zeros as bandwidth enhancers, shunt-series amplifier, f_i doublers, neutralization and unilateralization

Need for LNA: Friis’ equation - Low noise amplifier design – LNA topologies: noise cancelling LNA topology, distortion cancelling LNA topology - linearity and large signal performance


RF power amplifiers – Class A, AB, B, C, D, E and F amplifiers, modulation of power amplifiers, linearity considerations. RFIC simulation and layout- General Layout Issues, Passive and Active Component Layout.

Text Books

Reference Books

Course outcomes
At the end of the course student will be able to
CO1: understand the basics of RF system design and analyse the high frequency amplifier design
CO2: appreciate the need for LNA and learn different LNA topologies and design techniques
CO3: understand the requirement of RF Mixer, its function and performance parameters
CO4: analyse the various types of synthesizers, oscillators and their characteristics.
CO5: learn about the need for power amplifiers and the effects of nonlinearities
Course Learning Objective

- To expose the students to all aspects of functional verification of digital systems

Course Content

System Verilog (SV) - Data Types, Arrays, Structures, Unions, Procedural Blocks, Tasks and Functions, Procedural Statements, Interfaces, Basic OOPs, Randomization, Threads and Inter Process Communication, Advanced OOPs and Test bench guidelines, Advanced Interfaces.

A Complete System Verilog Test Bench (SVTB), Functional Coverage in System Verilog, Interfacing with C, FSM Modelling with SV, Connecting Test bench and Design, Behavioral and Transaction Level Modelling with SV

System Verilog Assertions (SVA) – Introduction to SVA, Building blocks, Properties, Boolean expressions, Sequence, Single and Multiple Clock definitions, Implication operators (Overlapping and Non-overlapping), Repetition operators, Built-in System functions ($past, $stable, $onehot, $onehot0, $isunknown), Constructs (ended, and, intersect, or, first_match, throughout, within, disableiff, expect, matched, if –else), assertion directives, nested implication, formal arguments in property.

SVA using local variables, calling subroutines, SVA for functional coverage, Connecting SVA to the Design or Test bench, SVA for FSMs, Memories, Protocol checkers, SVA Simulation Methodology, Assertions: Practice and Methodology, Re-use of Assertions, Tracking coverage with Assertions, Using SVA with other languages.


Text Books


Reference Books

3. Recent literature in Functional Verification using Hardware Verification Languages.

Course outcomes

At the end of the course student will be able to
CO1: To learn about the testing environment of digital systems
CO2: To create test benches for digital systems
CO3: To learn about verification methodologies
CO4: To understand the need for system verification
CO5: To acquire digital verification skills
Course Code : EC676
Course Title : Testability of Analog / Mixed-Signal Circuits and High Speed Circuit Design
Number of Credits : 3
Course Type : Elective

Course Learning Objective
- To expose the students to all aspects of testing analog/mixed-signal circuits.

Course Content

ADC Testing: ADC testing versus DAC testing, DC tests and Transfer curve tests, Dynamic ADC tests, ADC Architectures. Sampling Theory. DSP based testing: Advantages of DSP based testing, DSP, Discrete-time transforms, The Inverse FFT.


High speed design techniques: High Speed Op-amps, High Speed op-amp applications, RF/IF Subsystems.

High Speed sampling and High Speed ADCs, High Speed DACs and DDS systems.

Text Books
1. An Introduction to Mixed-signal IC test and Measurement - Mark Burns, Gordon W. Roberts
2. High Speed Design Techniques - Walt Kester, Analog Devices

Reference Books
2. The Fundamentals of Mixed Signal Testing - Brian Lowe
3. Test and Design for Testability in Mixed Signal ICs - Jose L Huertas
5. Recent literature in Testability of Analog / Mixed-Signal Circuits and High Speed Circuit Design.

Course outcomes
At the end of the course student will be able to
CO1: To understand the testing methodology
CO2: To build test systems
CO3: To understand the requirements for BIST
CO4: To learn about error correction mechanisms
CO5: To understand the benefits of BIST
Course Code : EC677
Course Title : High Speed System Design
Number of Credits : 3
Course Type : Elective

Course Learning Objective
- To expose the students to all aspects of electronic packaging including electrical, thermal, mechanical and reliability issues.

Course Content
Functions of an Electronic Package, Packaging Hierarchy, IC packaging: MEMS packaging, consumer electronics packaging, medical electronics packaging, Trends, Challenges, Driving Forces on Packaging Technology, Materials for Microelectronic packaging, Packaging Material Properties, Ceramics, Polymers, and Metals in Packaging, Material for high density interconnect substrates

Overview of Transmission line theory, Clock Distribution, Noise Sources, power Distribution, signal distribution, EMI; crosstalk and nonideal effects; signal integrity: impact of packages, vias, traces, connectors; non-ideal return current paths, high frequency power delivery, simultaneous switching noise; system-level timing analysis and budgeting; methodologies for design of high speed buses; radiated emissions and minimizing system noise.


Text Book

Reference Books
6. Recent literature in Electronic Packaging.

Course outcomes
At the end of the course student will be able to
CO1: design of PCBs which minimize the EMI and operate at higher frequency.
CO2: design of packages which can withstand higher temperature, vibrations and shock.
CO3: explain the basic techniques for statistical process control and failure mode and effect analysis.
CO4: prescribe and perform parametric test and analysis and the troubleshooting of electronic circuits with the application of basic and virtual electronic instruments
CO5: explain contemporary pragmatic manufacturing processes, interconnects and assembly methods for electronic equipment fabrication.
Course Code : EC678
Course Title : Modelling of Solid-State Circuits
Number of Credits : 3
Course Type : Elective

Course Objectives
- To study and model MOS Transistors and MOS Capacitors
- To understand the various CMOS design parameters and their impact on performance of the device.
- To study the device level characteristics of BJT transistors

Course Content
Surface Potential: Accumulation, Depletion, and Inversion, Electrostatic Potential and Charge Distribution in Silicon, Capacitances in an MOS Structure, Polysilicon-Gate Work Function and Depletion Effects, MOS under Non-equilibrium and Gated Diodes, Charge in Silicon Dioxide and at the Silicon–Oxide Interface, Effect of Interface Traps and Oxide Charge on Device Characteristics, High-Field Effects, Impact Ionization and Avalanche Breakdown, Band-to-Band Tunnelling, Tunnelling into and through Silicon Dioxide, Injection of Hot Carriers from Silicon into Silicon Dioxide, High-Field Effects in Gated Diodes, Dielectric Breakdown

Long-Channel MOSFETs, Drain-Current Model, MOSFET I–V Characteristics, Subthreshold Characteristics, Substrate Bias and Temperature Dependence of Threshold Voltage, MOSFET Channel Mobility, MOSFET Capacitances and Inversion-Layer Capacitance Effect, Short-Channel MOSFETs, Short-Channel Effect, Velocity Saturation and High-Field Transport Channel Length Modulation, Source–Drain Series Resistance, MOSFET Degradation and Breakdown at High Fields.


Common-Base Current Gain in the Presence of Base–Collector Junction Avalanche, Saturation Currents in a Transistor, Relation Between $B_{VCEO}$ and $B_{VCBO}$.

Reference Books:

Course outcomes
At the end of the course student will be able to
CO1: To design and model MOSFET and BJT devices to desired specifications.
CO2: To understand the physics behind the device operation
CO3: To analyse the impact of the device physics in circuit design
CO4: To model novel semiconductor devices
CO5: To analyse the working of deep submicron semiconductor devices.
Course Code : EC679
Course Title : Nano-Scale Devices: Modelling and Circuits
Number of Credits : 3
Course Type : Elective

Course Objectives
- To introduce novel MOSFET devices and understand the advantages of multi-gate devices
- To introduce the concepts of nanoscale MOS transistor and their performance characteristics
- To study the various nano-scaled MOS transistor circuits

Course Content


Radiation effects in SOI MOSFETs, total ionizing dose effects – single-gate SOI – multi-gate devices, single event effect, scaling effects


Reference Books:

Course Outcomes
At the end of the course student will be able to
CO1: study the MOS devices used below 10nm and beyond with an eye on the future
CO2: understand and study the physics behind the operation of multi-gate systems.
CO3: design circuits using nano-scaled MOS transistors with the physical insight of their functional characteristics
CO4: To appreciate the growth of scaling in MOSFETs
CO5: To understand the physical effects in deep sub-micron MOS devices
Course Code: EC680
Course Title: Embedded System Design
Number of Credits: 3
Course Type: Elective

Course Objective
- Ability to understand the technologies and techniques underlying in developing an embedded system.

Course Content
Introduction to Embedded system, embedded system examples, Parts of Embedded System
Typical Processor architecture, Power supply, clock, Cache memory, memory interface, interrupt, I/O ports, Buffers, Programmable Devices, ASIC etc. Bus architecture - I²C, SPI, AMBA, CAN. Memory Technologies – EPROM, Flash, OTP, SRAM, DRAM, SDRAM etc.

Introduction to Cypress Programmable System on Chip (PSoC). Structure of PSoC, PSoC Designer, PSoC Modules, Interconnects, Memory Management, Global Resources, Design Examples

Basic Features of an Operating System, Kernel Features [polled loop system, interrupt driven system, multi rate system], Processes and Threads, Context Switching, Scheduling[RMA, EDF, fault tolerant scheduling], Inter-process Communication, real Time memory management [process stack management, dynamic allocation], I/O [synchronous and asynchronous I/O, Interrupts Handling, Device drivers], RTOS [ VxWorks, RT-LINUX].


Text Books

Course outcomes
At the end of the course student will be able to
CO1: define an embedded system and compare with general purpose system.
CO2: appreciate the methods adapted for the development of a typical embedded system.
CO3: get introduced to RTOS and related mechanisms.
CO4: To build embedded systems for real-time applications
CO5: To debug digital embedded systems and solve complex problems.
Course Objective

- To give an exposure on the infrastructure, sensor technologies and networking technologies of IoT.
- To analyse, design and develop IOT solutions.
- To apply the concept of Internet of Things in the real world scenarios.

Course Content


Clustering, Clustering for Scalability, Clustering Protocols for IOT.

The Future Web of Things – Set up cloud environment –Cloud access from sensors– Data Analytics for IOT- Case studies- Open Source ‘e-Health sensor platform’ – ‘Be Close Elderly monitoring’ – Other recent projects.

Text Books


Reference Book

1. Charalampos Doukas , “Building Internet of Things with the Arduino” Create space, April 2002
2. Dr. Ovidiu Vermesan and Dr. Peter Friess, “Internet of Things: From research and innovation to market deployment”, River Publishers 2014.

Course outcomes

At the end of the course student will be able to
CO1: identify the components of Internet of Things
CO2: development of IoT based application.
CO3: Build IoT based platforms for various use cases
CO4: Study the data gathered by IoT devices
CO5: Predict and dynamically optimize systems based on IoT data
Course Code : EC682  
Course Title : Semiconductor Memories  
Number of Credits : 3  
Course Type : Elective

Course Contents:

Memory hierarchy in digital systems; Static RAM: Types, Overall architecture, SRAM Cell - Design, Layout, Noise Issues and Margins and Assembly of Core, Peripheral Circuitry - Decoding, Array conditioning for read/write, Sensing, Writing, Synchronization;

Dynamic RAM: Types, Cell design, Assembly of core, Core architectures, Peripheral circuitry - Sensing, Elevated voltage supplies; Modern high speed DRAM - EDO, SDR, DDR;

Non Volatile Memories: ROM - Array Design, EPROM - Cell and Array Design, EEPROM - Tunnelling Phenomena, EEPROM Cell both Hot Carrier based operation and Tunnelling based Operation;

Flash Memories: Cell operation and design, Types of modern high density flash memories - NOR Flash, NAND Flash.

Reference Books:


Course outcomes
At the end of the course student will be able to

CO1: identify the parts of Memories
CO2: development of Semiconductor Memory architectures.
CO3: To learn the fundamental problems in memory design
CO4: develop novel circuit techniques for improving memory design
CO5: To understand and appreciate the growing semiconductor market for memory
Course Code: EC683
Course Title: FPGA Based System Design
Number of Credits: 3
Course Type: Elective

Course Learning Objective
- To enable the students to understand the design and performance measures of FPGA based system design

Course Content


Text Book

Reference Books

Course outcomes
At the end of the course student will be able to
CO1: acquire the basics of Multi rate Digital Signal Processing.
CO2: understand the concepts of Filter Banks and its applications.
CO3: understand the concepts and algorithms of Adaptive Filter theory.
CO4: understand the basics of Digital waveform synthesis and appreciate its applicability to various communication systems.
CO5: understand the concepts of Digital Down converters and Demodulators.
Course Code : EC684
Course Title : Bio-Medical CMOS ICs
Number of Credits : 3
Course Type : Elective

Course Learning Objective
- To develop skills to design biomedical IC circuits

Course Content


Readout circuits: Biopotential Acquisition, Power Efficient Instrumentation Amplifier Topologies for Biopotential Signal Extraction, Current Mode Instrumentation Amplifiers, Examples of ICs for Biopotential Acquisition.

Basic operation principles and architectures as well as the most recent research results of low power CMOS ICs. Low power ADCs for Bio-Medical Applications, Low Power Bio-Medical DSP.


Text Books

Reference Books

Course outcomes
At the end of the course student will be able to
CO1: familiarise the concepts of used to design biomedical ICs
CO2: acquire knowledge to design various electrodes
CO3: learn the design of various biomedical amplifiers
CO4: analyse and implement various low power ADCs for biomedical applications
CO5: acquire knowledge about types of short range wireless communication
Course Code : EC685  
Course Title : On-chip Antenna Design  
Number of Credits : 3  
Course Type : Elective

Course Learning Objective
- To make the students understand the basic concepts and design procedures of on-chip antennas.
- Introduce the students to various packaging technologies for on-chip antennas

Course Content
Introduction to millimetre wave technologies: Antenna, RF Electronics, Packaging, Millimetre wave packaging, Review of Microwave Packaging Technologies, Low-cost mm Wave Packaging, Emerging Packaging Technologies, Package Co-design at mm Waves.

Millimetre-wave Interconnects: Interconnects at Millimetre-wave Frequencies, Interconnect Technology Options for Millimetre-wave Applications, Performance-oriented Interconnect Technology Optimization, Chip-to-package Interconnects at Millimetre-wave Frequencies.


Text Books

Reference Books

Course outcomes
At the end of the course student will be able to
CO1: Familiarise the effects of substrates on millimetre wave antennas
CO2: Design of interconnects at millimetre wave frequencies
CO3: Design millimetre wave printed antennas antennas
CO4: Enable design of antennas with packages
CO5: Acquire knowledge about antenna arrays and phased arrays
Course Learning Objective

- To give an exposure to the various fixed point and floating point DSP architectures and to implement real time applications using these processors.

Course Content


Digital Media Processors. Video processing sub systems. Multi-core DSPs. OMAP. CORTEX, SHARC, SIMD, MIMD Architectures.

Text Books


Reference Books

4. Recent literature in DSP Architecture.

Course outcomes

At the end of the course student will be able to

CO1: learn the architecture details fixed and floating point DSPs
CO2: infer about the control instructions, interrupts, and pipeline operations, memory and buses.
CO3: illustrate the features of on-chip peripheral devices and its interfacing with real time application devices.
CO4: learn to implement the signal processing algorithms and applications in DSPs.
CO5: learn the architecture of advanced DSPs.
Course Code : EC613
Course Title : High Speed Communication Networks
Number of Credits : 3
Course Type : Elective

Course Learning Objective
- To impart the students a thorough exposure to the various high speed networking technologies and to analyze the methods adopted for performance modeling, traffic management and routing

Course Content
The need for a protocol architecture, The TCP/IP protocol architecture, Internetworking, Packet switching networks, Frame relay networks, Asynchronous Transfer mode (ATM) protocol architecture, High speed LANs. Multistage networks

Overview of probability and stochastic process, Queuing analysis, single server and multi-server queues, queues with priorities, networks of queues, Self similar Data traffic

Congestion control in data networks and internets, Link level flow and error control, TCP traffic control, Traffic and congestion control in ATM networks

Overview of Graph theory and least cost paths, Interior routing protocols, Exterior routing protocols and multicast.

Quality of service in IP networks, Integrated and differentiated services, Protocols for QOS support-Resource reservation protocol, Multiprotocol label switching, Real time transport protocol.

Text Books

Reference Books
3. Recent literature in High Speed Communication Networks.

Course outcomes
At the end of the course student will be able to
CO1: compare and analyze the fundamental principles of various high speed communication networks and their protocol architectures
CO2: analyze the methods adopted for performance modeling of traffic flow and estimation
CO3: examine the congestion control issues and traffic management in TCP/IP and ATM networks
CO4: compare, analyze and implement the various routing protocols in simulation software tools
CO5: examine the various services.
Course Code : EC615
Course Title : Digital Image Processing
Number of Credits : 3
Course Type : Elective

Course Learning Objective
- To explore various techniques involved in Digital Image Processing.

Course Content


Feature Extraction from the Image: Boundary descriptors, Regional descriptors, Relational descriptors. Dimensionality reduction techniques, Discriminative approach and the Probabilistic approach for image pattern recognition.

Text Books

Reference Books
3. E.S.Gopi, ”Digital Image processing using Matlab”, Scitech publications, 2005
4. Recent literature in Digital Image Processing.

Course outcomes
At the end of the course student will be able to
CO1: understand the need for image transforms different types of image transforms and their properties.
CO2: develop any image processing application.
CO3: understand the rapid advances in Machine vision.
CO4: learn different techniques employed for the enhancement of images.
CO5: learn different causes for image degradation and overview of image restoration techniques.
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<tr>
<th>Course Code</th>
<th>: EC616</th>
</tr>
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<tbody>
<tr>
<td>Course Title</td>
<td>: RF MEMS</td>
</tr>
<tr>
<td>Number of Credits</td>
<td>: 3</td>
</tr>
<tr>
<td>Course Type</td>
<td>: Elective</td>
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</tbody>
</table>

**Course Learning Objective**

- To impart knowledge on basics of MEMS and their applications in RF circuit design.

**Course Content**


Micro-machined transmission lines. Coplanar lines. Micro-machined directional coupler and mixer.


**Text Book**


**Reference Books**

3. Recent literature in RF MEMS.

**Course outcomes**

At the end of the course student will be able to

CO1: learn the Micromachining Processes

CO2: learn the design and applications of RF MEMS inductors and capacitors.

CO3: learn about RF MEMS Filters and RF MEMS Phase Shifters.

CO4: learn about the suitability of micro-machined transmission lines for RF MEMS.

CO5: learn about the Micro-machined Antennas and Reconfigurable Antennas.
Course Code : EC626
Course Title : Bio MEMS
Number of Credits : 3
Course Type : Elective

Course Learning Objective
- To train the students in the design aspects of Bio MEMS devices and Systems. To make the students aware of applications in various medical specialists especially the Comparison of conventions methods and Bio MEMS usage.

Course Content
Introduction-The driving force behind Biomedical Applications – Biocompatibility - Reliability Considerations-Regularity Considerations – Organizations - Education of Bio MEMS-Silicon Micro fabrication-Soft Fabrication techniques


SENSOR PRINCIPLES and MICRO SENSORS: Introduction-Fabrication-Basic Sensors-Optical fibers-Piezo electricity and SAW devices-Electrochemical detection-Applications in Medicine


Text Book


Reference Books

6. Recent literature in Bio MEMS.

Course outcomes
At the end of the course student will be able to
CO1: learn and realize the MEMS applications in Bio Medical Engineering
CO2: understand the Micro fluidic Principles and study its applications.
CO3: learn the applications of Sensors in Health Engineering.
CO4: learn the principles of Micro Actuators and Drug Delivery system
CO5: learn the principles and applications of Micro Total Analysis