

REGISTRATION AND CERTIFICATION

- Maximum seats: 25 (selection based on merit and first come, first serve basis)
- No Registration Fee
- Online registration form link:
<https://forms.gle/Lg4Gd7FHCMhiPoLPA>
- Please fill the above Google form with the requested details and upload the scanned copies of the certificate, resume, and declaration form along with NOC (from the Project supervisor/HoD/Head of the institution) by 17th May 2023.
- The applications will be screened, and the candidates will be selected on merit. The selection committee's decision will be final in the selection of candidates.
- The selected candidates will be informed by email on or before 25th May 2023.
- The selected candidates will have to acknowledge participating in the workshop through return email (on or before 01st June 2023), failing which the waitlisted candidates may be called to attend the workshop.
- Certificates will be provided to the participants after the successful completion of the workshop.
- Selected participants will be accommodated in Institute guest house/hostel rooms (if available) with catering facilities under the funds approved by SERB (as per norms).
- The participating students will be eligible for TA reimbursement for their journey to the host institute from their home town/home institute, both ways, as per the GoI norms.

IMPORTANT DATES

Last date of registration: 17/05/2023
List of selected students: 25/05/2023
Last date to accept the offer: 01/06/2023

Participants: Eligibility Criteria

- Only regular PG level (i.e., Masters or Ph.D.) students pursuing their degree from AICTE approved Institution within India are eligible to apply.
- Relevant areas of specialization include (but are not limited to): Embedded Systems, VLSI based system design, On-Chip Networks, FPGA Implementation.
- The applicants should produce a declaration form and a "No Objection Certificate (NOC)" from the Supervisor/Head of the Department/ Institute, allowing their student to undergo training in the workshop if selected.

CHIEF PATRON & CHAIRMAN

Dr. G. Aghila

Director, NIT Tiruchirappalli

PATRON

Prof. G. Lakshmi Narayanan

Department of ECE., NIT Tiruchirappalli

CO-CHAIRMAN

Dr. M. Bhaskar, HoD

Department of ECE, NIT Tiruchirappalli

ADDRESS FOR CORRESPONDENCE

Dr. B. Naresh Kumar Reddy,

Assistant Professor, ECE

National Institute of Technology Tiruchirappalli
Tiruchirappalli, Tamil Nadu- 620015

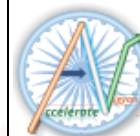
Email: bnkreddy@nitt.edu

Contact Number: +91- 9966539090

Further details:

Contact: Mr. T. Nikhil Kumar (+91-6281110917)

Mr. Shaik Sameer (+91-6302871550)



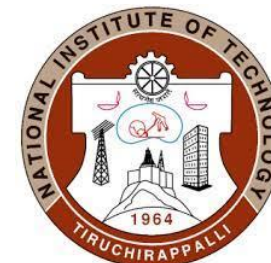
ACCELERATE
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SERB Sponsored

**One Week High-End Workshop on
Hands-on Training on FPGA
Architectures and Programming
using Verilog HDL
[Physical Mode]**

(05th to 11th June 2023)



EVENT ORGANIZER

Dr. B. Naresh Kumar Reddy, Assistant Professor

COORDINATORS

Dr. Srinivasulu Jogi, Assistant Professor,

Dr. B. Chandrababu Naik, Assistant Professor,

Organized by:

**Department of Electronics and
Communication Engineering,
National Institute of Technology
Tiruchirappalli, Tiruchirappalli,
Tamilnadu-620015.**

Venue: Dept. of Electronics and Communication Engineering, NIT Tiruchirappalli

Accommodation: A limited number of rooms in NITT Guest house/Hostels are available on First Come, and First Served basis. THE HOST INSTITUTION SHALL BEAR the boarding and lodging within the NITT premise only (from the SERB fund). If unavailable, the participants need to make self-arrangements for their stay outside the NITT premise, which the organizers do not bear. TA will be reimbursed for the train or bus lowest fare.

About the Institute

National Institute of Technology (formerly known as Regional Engineering College) Tiruchirappalli is one among the premier Institutions of India and is well known for its high standards in teaching and research. It offers 10 undergraduate and 23 postgraduate programs in disciplines spanning engineering, science, architecture, and management. It has been declared as an Institute of National Importance by the Government of India under NIT Act. NIT Tiruchirappalli retained its No. 1 position among all NITs, 6th year in a row in the “India Rankings 2021” released by NIRF. The Institute has signed MoUs with various Industries and Institutions both in India as well as in abroad to promote collaborative research and consultancy.

About the Department

The Electronics and Communication Engineering (ECE) Department was established in the year 1968. The department offers Undergraduate (UG), Postgraduate (PG), M.S. (By Research) and Ph.D.,

degree programs that provide students with the knowledge and tools they need to succeed in the Electronics and Communication Engineering. Research in the department focuses on high-impact various disciplines: Communication systems, Wireless networks, Signal and Image Processing, RF MEMS and MIC, Microwave antennas, Optical communication and Photonics, VLSI technologies. Many of our Ph.D. graduates have taken up faculty positions in other NITs and IITs.

About the Karyashala Scheme

KARYASHALA is a program offered by the Science and Engineering Research Board (SERB), Government of India, via Accelerate Vigyan scheme to boost Research & Development in the country by enabling and grooming potential PG level students (masters and Ph.D. students) by developing dedicated research skills in selected areas/disciplines through high-end workshops. This program aims to provide opportunities to acquire specialized research skills.

About the Workshop

Programmable Logic Design has become a core technology utilized in building electronic systems. By integrating soft-core or hardcore processors, these devices have evolved to complete systems on a chip, steadily augmenting or even displacing general purpose processors. In particular, high-performance computing is mostly archived with FPGAs.

This workshop is intended to give participants a quick start and hands on practice needed for implementing cutting edge projects. Hence, a workshop on a FPGA Architectures using Verilog shall be helpful to potential Ph.D./M.Tech students.

This workshop shall focus on a recent trend in FPGA implementation of digital circuits and various architectures. Overall, this workshop shall serve to be an excellent platform for upgrading the participants' knowledge in the domain of FPGA applications to digital circuits and various architectures.

Objectives of the Workshop:

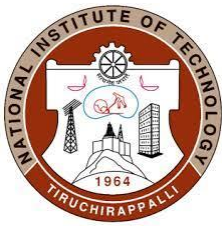
- To understand FPGA architectures and how they can be used to implement digital circuits.**
- To use Verilog HDL to model and design digital circuits and systems.**
- To use design tools and software to implement and test digital circuits on FPGAs.**
- To debug and troubleshoot digital circuits and systems.**

Course Contents:

- Introduction to VLSI design flow**
- RTL design (Verilog HDL) quick start**
- Combinational circuits and sequential circuits using FPGA**
- Synchronous and Asynchronous circuits using FPGA**
- Delays and Clock in Verilog, FSM Coding**
- Implementation of different Digital circuits using FPGA.**
- FPGA Architectures and FPGA Design Flow.**
- Advanced FPGA topics.**
- FPGA based SoC Design-Case study.**

Resource Persons

Subject experts from prestigious academic institutions (like IITs, NITs, etc.), R&D organizations, and industries will deliver the workshop contents. The coordinators and student volunteers will mentor the hands-on sessions.



**One Week High-End Workshop on
Hands-on Training on FPGA Architectures and Programming
using Verilog HDL
[Physical Mode]**

DECLARATION FORM

1. Name (In Block Letters):
 2. Date of birth:Gender:
 3. Category (M.Tech/M.E/M.S./Ph.D. student):
 4. Institution:
 5. Department:
 6. Mobile:
 7. e-mail:
 8. Specialization:
 9. Accommodation is required (Yes/No).....
 10. Official Address:
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Declaration: The information provided is true to the best of my knowledge. If selected, I agree to abide by the rules and regulations of the program and shall attend the course for the entire duration.

Name & Signature of the candidate

No Objection Certificate (NOC) from Project Supervisor/HoD/Head of Institution

I hereby certify that Mr./Ms. is a
..... (M.Tech/M.E/PhD) student of
..... I have no objection to him/her undergoing a high-end
workshop (if selected) on “**Hands-on Training on FPGA Architectures and Programming
using Verilog HDL**” at the National Institute of Technology Tiruchirappalli, Tamil Nadu,
from **05th to 11th June 2023**.

Place:

Name & Signature of Project
Supervisor/HoD/Head of Institution

Date:

(Department/Institute Seal)