National Institute of Technology, Tiruchirappalli: Performa for CV of Faculty/ Staff Members

Curriculum Vitae

Dr. M.Bhaskar, Professor, Department of Electronics and Communication Engineering, National Institute of Technology, Tiruchirappalli-15, completed B.E. degree in Electronics and communication Engineering, M.E. in Microwave and Optical Engineering and Ph.D. in VLSI Design. Having 29 years of teaching experience and 21 years of research experience and taught 20 theory courses and 6 laboratory courses in the under graduate level and 5 theory courses and one laboratory course in the post graduate level. Guided 26 UG projects, 69 PG projects; four Ph.D. scholars completed their Degree and six more in progress in the area of VLSI Design and Signal Processing. Mentored 10 internship projects and supervised five research projects.

More fascinated to do hardware based real time projects, publications include 31 Journal papers, 34 international conference papers and 7 national conference papers and one book 'Digital Signal Processors and Application' in Tata McGraw Hill. Won many best paper awards and attended large number of workshops, training programs and conferences.

Areas of research are VLSI System Design, Low Power VLSI Design, On-chip wireless transceivers, On-chip antenna design, Digital Signal Processor Architectures, Signal processing algorithm Implementation in DSPs, Embedded System Design, VLSI implementation of Biomedical Algorithms and Internet of Things (IoT) System Design

Expertise in the purchase, installation and operation of various equipment and software for the various laboratories. In addition, skills in purchase, installation and maintenance of telephone exchanges, cable TV networks, community FM station and all IT infrastructures equipment and systems.

1. Name : **Dr. M.Bhaskar**

2. Designation : **Professor**

3. Office Address : **Department of Electronics & Communication Engineering National Institute of Technology, Tiruchirappalli – 620 015**

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5. Email (Primary): **bhaskar@nitt.edu**   Email (Secondary) : **bhaskar_72@rediffmail.com**

6. Field(s) of Specialization:

   1. **VLSI System Design,**
   2. **Low Power VLSI Design**
   3. **On-chip wireless transceivers,**
   4. **On-chip antenna design**
   5. **DSP Architectures,**
   6. **Signal processing algorithm Implementation in DSPs.**
   7. **Embedded System Design**
   8. **VLSI implementation of Biomedical Algorithms**
   9. **IoT System Design**

7.   Employment Profile

Job Title	Employer	From	To
Professor	National Institute of Technology Tiruchirappalli – 620 015	March 2018	Till date
Associate Professor	National Institute of Technology Tiruchirappalli – 620 015	July 2010	March 2018
Lecturer Selection Grade (SG)	National Institute of Technology Tiruchirappalli – 620 015	July 2007	July 2010
Lecturer Senior scale (SL)	National Institute of Technology Tiruchirappalli – 620 015	May 2002	July 2007
Lecturer	Regional Engineering College Tiruchirappalli – 620 015	May 1997	May 2002
Lecturer	Shanmugha College of Engineering, Thanjavur	June 1995	April 1997
Project Trainee	ISRO, Antenna Division, Bangalore	August 1994	January 1995
Part-time teacher	Govt. College of Engineering, Salem	Sept. 1992	Sept 1993

8. Academic Qualifications (From Highest Degree to High School):

Examination	Board / University	Year	Division/ Grade	Subjects
Ph.D.	National Institute of Technology Tiruchirappalli – 620 015	2015	-	VLSI Design
M.E.	Madurai Kamaraj University Alagappa Chettiyar Govt. College of Engineering, Karaikudi - 630 003	1995	I Class with Distinction	Microwave and Optical Engineering
B.E.	Bharathiyar University Kongu Engineerg College Perundurai Erode – 638 060	1992	I Class	Electronics and Communication Engineering
H.S.C	H.S.C Board	1988	I Class	Mathematics and Science
S.S.L.C	S.S.L.C. Board	1986	I Class (School First)	Mathematics and Science

9. Academic/Administrative Responsibilities within the University

S. No.	Position	Faculty/Department/Centre/Institution	From	To
1.	Head of the Department	Electronics and Communication Engineering Department	2023	Till date
2.	Head of the Department	Computer Support Group (CSG)	2020	2022
3.	Convener	NIT Community Radio station FM 90.8	2019	Till date

4.	Broadcasting coordinator	NIT Community Radio station FM 90.8	2016	2019
5.	Convener	Campus Communication Services (CCS)	2016	2020
6.	Additional Convener	Campus Communication Services (CCS)	2001	2016
7.	Coordinator	Centre for Electronic System Design, Calibration and Testing (HEFA)	2020	Till date
8.	Lab-in-charge	ECE-DSP laboratory	2000	Till date
9.	Lab-in-charge	RF IC Design Research Laboratory	2016	Till date
10.	Nodal Center Coordinator	Smart India Hackathon (SIH) Grand Finale, Organized by MHRD and AICTE. 2019	Hardware edition 8-12 July 2019	
11.	Nodal Center Coordinator	Smart India Hackathon (SIH) Grand Finale, Organized by MHRD and AICTE. 2019	Software edition 2-3 March 2019	
12.	Nodal Center Coordinator	Smart India Hackathon (SIH) Grand Finale, Organized by MHRD and AICTE. 2018	Hardware edition 18-22 June 2018	
13.	Member of Convocation Committee, Infrastructure	NIT, Trichy	2020	Till date
14.	Member of Institute day Committee, Video and Photography	NIT, Trichy	2020	Till date
15.	Coordinator, UG and PG Syllabus update	ECE, NIT, Trichy	2000	2015
16.	Member of Telephone and Cable TV network committee	Campus Communication Services (CCS), NIT, Trichy	1998	2001
17.	Member of library committee	NIT, Library	2003	2005
18.	Member of audio visual committee	NIT, Trichy	2003	Till date
19.	Member of quality assurance committee for Estate office	NIT-Estate office	2007	2010
20.	Member of video conference establishment committee	NIT-CSE dept.	2008	2009
21.	Member of purchase committee audio system equipment purchase to various halls of the institute	NIT, Trichy	2007	2012
22.	Member of Project team in Digital classroom setup.	NIT, Trichy	2015	2018
23.	Member of IoT lab governing council	NIT-1981 Alumni setup IoT lab	2015	Till date

10. Academic/Administrative Responsibilities outside the University

S. No.	Position	Institution	From	To
1	Member, Board of studies	KSR college of Eng., Tiruchengode	2012	2020
2	Member, Board of studies	Govt. college of Eng., Salem	2014	2018
3	Member, Doctoral Committee	Vellore Institute of Technology, Vellore	2015	Till date
4	Member, Board of studies	Govt. college of Technology, Coimbatore	2016	2018

11. Awards, Associateships etc.

S. No.	Year of Award	Name of the Award	Awarding Organization
1	1998	Second prize in the DSP Design contest	IISc, Bangalore
2	2009	Best paper award	ICOICT 2009, International conference
3	2010	Best paper award	NCVESCOM 2010, 3rd National Conference on VLSI
4	2011	3rd position in the Young Scientist category	ICSCCN 2011, International conference
5	2014	Best paper award	MICRO-2014 1st International conference on Microelectronics

12. Fellowships

Year of Award	Name of the Fellowship	Awarding Organization	From (Month/Year)	To (Month/Year)
	NIL			

13. Details of Academic Work

(i)   Curriculum Development
   1. Periodically updated the syllabus for the following courses
    i) DSP architectures and applications (UG)
    ii) Introduced new UG Elective course Internet of Things (IoT) in 2019
    iii) Low power VLSI Circuits (UG)
    iv) Low Power VLSI Systems (PG)
    v) DSP Architectures (PG)
   2. Periodically updated the experiments for Digital Signal Processing laboratory course both for UG and PG.
   3. Purchased latest equipments for the Signal Processing laboratory
   4. Established a new Research Laboratory 'RF IC Design Laboratory
   5. Establish a new Centre 'Centre for Electronics System Design, Calibration and Testing' under HEFA in 2019

(ii)   Courses taught at Postgraduate and Undergraduate levels
Undergraduate Level

Theory courses	Laboratory Courses
1. Semiconductor physics and devices 2. Engineering Electromagnetics 3. Transmission lines and wave guides 4. Digital electronics 5. Signals and systems 6. Communication electronic circuits 7. Digital signal processing 8. Digital signal processor architectures and Applications 9. Applied electronics 10. Internet of Things (IoT) 11. Low Power VLSI Circuits	1. Electronic devices lab 2. Communication lab 3. Digital signal processing lab

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Postgraduate Level

Theory courses	Laboratory Courses
1. Analog VLSI circuits 2. Low power VLSI Systems 3. DSP Architectures	1. Digital signal processing lab

(iii)   Projects guided at Undergraduate and Postgraduate level
         B.Tech. Projects guided - 26
         M.Tech. Projects guided - 69
         M.Sc.   Projects guided - 2

(iv)   Other contribution(s)
         1. The Signal Processing Laboratory was established from scratch in SJB building 2nd floor in 2011.
         2. As a Member of purchase committee, purchased the desktop computers for various laboratories from 2002 to 2015.

14. Details of Major R&D Projects

Title of Project	Funding Agency	Duration		Status
		From	**To**	**Ongoing/ Completed**
Design and development of 14-bit 10 MSPS 50mW SAR ADC	ISRO, Respond Co-PI	2019	2022	Completed
Wireless Transceiver for Low data rate applications	Deity, New Delhi C2SD/ SMDP-III - PI	2015	2020	Completed

Design & implementation of baseband modules for wireless sensor networks	Broadcom Foundation, USA – Co-PI	2015	2017	Completed
Design and implementation of Low power analog front end modules for wireless sensor networks	Deity, New Delhi Co-PI	2012	2015	Completed
Modernization of Signal Processing Laboratory	MODROB, DST - PI	2003	2005	Completed

15. Number of PhDs guided

Name of the PhD Scholar	Title of PhD Thesis	Role(Supervisor/ Co-Supervisor)	Year of Award
Archana S.	Co-Design and analysis of On-Chip Antennas with Power Amplifier and Low Noise Amplifier	Supervisor	2020
Chrisben Gladson S	Power-Efficient Linearity Improvement Techniques for Radio Frequency Mixer Circuits	Supervisor	2020
Arunkumar K R	De-Noising Techniques for Heart Rate Estimation from PPG Signals	Supervisor	2020
Lakshmi N.S.	Design of Gyrator-C Based Active Inductor and Its use in the Design of Band pass Filter and Voltage-Controlled Oscillator	Supervisor	2022

16. Participation in Workshops/ Symposia/ Conferences/ Colloquia /Seminars/ Schools etc. (mentioning the role)

S. No.	Date (s)	Title of Activity	Level of Event	Role	Event Organized by	Venue
1	15.07.1996 – 19-07-1996	Training course on 'CP525/526 Communication Processors'	National	Participant	Siemens Advanced Training Institute	Mumbai
2	07.08.1998 – 18.08.1998	Instruction enhancement programme on 'Designing with Digital Signal Processing'	National	Participant	Indian Institute of Science	Bangalore
3	02.12.2002 – 13-12-2002	Winter school on 'Architecture, Programming and Applications of Digital Signal Processors'	National	Participant	Department of ECE, REC, Trichy	Trichy
4	06.09.2004 – 10.09.2004	Short Term course under QIP on 'Digital VLSI Front end Design'	National	Participant	Department of Computer Science, IIT Madras	Chennai

5	13.09.2004 – 17.09.2004	AICTE-ISTE Short Term course on 'Advanced aspects of VLSI Design Automation'	National	Participant	Department of Computer Science, IIT Madras	Chennai
6	05.08.2005 - 06.08.2005	Workshop on 'Micro Electro Mechanical Systems (MEMS)'	National	Participant	Department of ICE, NIT, Trichy	Trichy
7	23.12. 2005 - 24.12. 2005	Workshop on 'Designing Systems on Programmable Chip (SOPC)'	National	Participant	Department of ECE, NIT, Trichy	Trichy
8	06.12. 2006 - 08.12. 2006	Training programme on 'Multi-Core Programming for Academia'	National	Participant	Intel Technology India Pvt. Ltd	Bangalore
9	29.12.2006 - 31.12.2006	Workshop on 'VLSI Implementation of Digital Radio Transceivers'	National	Participant	Department of ECE, NIT, Trichy	Trichy
10	04.01. 2007	Pre-Conference Tutorial on 'Embedded System on Chip'	National	Participant	International Conference TIMA 2007, NIT, Trichy	Trichy
11	12.02.2007 – 17.02.2002	Short term course under QIP on 'Analysis of Network Protocols and Design of Network Processor'	National	Participant	Department of CSE, NIT, Trichy	Trichy
12	07.03.2007 - 08.03.2007	Vendor's Workshop on 'Signal Processing System' Automation' under SMDP-II	National	Participant	Department of Electrical Engineering, IIT Madras	Chennai
13	13.12.2007 - 14.12.2007	2nd International Workshop on 'Interconnect Design and Variability'	National	Participant	VLSI Society of India	Bangalore
14	19.02.2009	Training Program on 'Computer Networking-Hardware and Software'	National	Participant	Department of CSE, NIT, Trichy	Trichy
15	12.03.2009 - 13.03.2009	Training program on 'Practical Aspects of Computer Networking'	National	Participant	Department of CSE, NIT, Trichy	Trichy
16	28.05.2015 – 29.05.2015	TEQIP – II sponsored 'Conclave on Academic Reforms'	National	Participant	NIT, Trichy	Trichy
17	31.10.2015	Workshop on 'Aspects of Analog and RF Test'	National	Participant	Texas Instruments, India	Bangalore

Conference Attended

S. No.	Date (s)	Title of Activity	Level of Event	Role	Event Organized by	Venue
1	19.11. 2008 – 21.11.2008	TENCON 2008	International Conference	Participant	IEEE Region 10	Hyderabad

2	26.02.2009 – 27.02.2009	ICOICT 2009	International Conference	Participant	Sri Chitra Thirnal College of Eng.	Trivandrum
3	08-01.2010 – 09.01.2010	ICRAES 2010	International Conference	Participant	K.S.R. College of Engineering	Tiruchengode
4	07.07. 2011- 09.07.2011	VDAT – 2011	National Symposium	Participant	VLSI Society of Indiaat Wipro Technologies	Pune
5	21.07. 2011 – 22-07.2011	ICSCCN 2011	International Conference	Participant	Noorul Islam Centre for Higher Education	Nagercoil
6	11.07. 2014 – 13.07.2014	MICRO-2014,	International Conference	Participant	IEEE EDS and IETE, Kolkata chapters	Kolkata

Conference chaired

S. No.	Date (s)	Title of Activity	Level of Event	Role	Event Organized by	Venue
1	11.07.2014 - 12.07.2014	1st International conference on Microelectronics, circuits and systems	International conference	Chairman	IEEE EDS and IETE, Kolkata chapters	Kolkata

17. Workshops/ Symposia/ Conferences/ Colloquia/Seminars Organized (as Chairman/ Organizing Secretary/ Convener / Co-Convener)

S. No.	Title of Activity	Level of Event	Date (s)	Role	Venue
1	Continuing education programme on 'Digital Signal Processor Programming and Applications	Local	08.06.1998 – 24.06.1998 12.06.2000 – 28.06.2000 24.11.2000 – 10.12.2000 15.06.2001 – 30.06.2001 30.11.2001 – 15.12.2001	Co. Coordinator	NIT, Trichy
2	Winter school on 'Architecture, Programming and Applications of Digital Signal Processors' sponsored by ISTE, New Delhi.	National	02.12.2002 – 13.12.2002	Co. Coordinator	NIT, Trichy

18. Invited Talks delivered

S. No.	Topic	Date	Inviting Organization
1	FDP-Architectures of TMS320C54X DSP and Applications	25.05.2016	Sri Krishna College of Engineering and Technology, Coimbatore
2	TEQIP sponsored work shop-	07.05.2016	TEQIP sponsored work shop on Evolution

	High Speed System Design		of 5G, Dept. of ECE, NIT, Trichy
3	AICTE sponsored QIP- Low Power VLSI Circuits	23.04.2016	Coimbatore Institute of Technology, Coimbatore
4	TEQIP-II sponsored FDP- Advanced DSP Processor Architectures for Signal Processing	11.12.2013	Anna University, BIT Campus, Trichy
5	Workshop- Digital Signal Processing and its applications	28.08.2010	K.L.N. College of Engineering, Madurai.
6	UGC sponsored seminar – Advances in Microprocessors and Microcontrollers	12.02.2010	SRC Autonomous college, Trichy
7	AICTE-ISTE sponsored STTP - Recent Trends in Signal Processing	15.02.2007	K.S.R. College of Engineering, Tiruchengode.
8	Invited talk - Digital Signal Processor under TEQIP	12.01.2007	Govt. College of Engineering, Salem.
9	Workshop – TMS320C50 and TMS320C54X processors	14.11.2006	Thanthai Periyar Govt. Institute of Technology, Vellore.

19. Membership of Learned Societies

S. No.	Type of Membership (Ordinary Member/ Honorary Member / Life Member)	Organization	Membership No. with date
1	Life Member	ISTE	LM31302 (2001)
2	Member	IETE	M189096 (12.01.2007)
3	Member	IEEE	93401280 (2016)

20. Academic Foreign Visits

Country	Duration of Visit	Programme
	Nil	

21. Publications

a) Refereed Research Journals:

S. No.	Author(s)	Title of Paper	Journal	Volume (No.)	Page Nos.	Year	Impact Factor
1.	Thenmozhi V, Bhaskar M	A 60-GHz low-noise amplifier with +7.258-dBm third-order input intercept point using current reuse feed forward distortion cancellation for 5G emerging communication	**Wiley**, International Journal of Circuit Theory and Applications	50	1855-1875	2022	2.378
2.	Thenmozhi V, Bhaskar M	Linearity improvement of LC cross-coupled low noise amplifier for X band applications	**Springer**, Microsystem Technologies	51	1-14	2022	2.012
3.	Lakshmi Nediyara	Current-Reuse Active	**Taylor and**	-	1-10	2022	2.333

	Suresh, Bhaskar Manickam	Inductor-Based VCO for Reconfigurable RF Front-End	**Francis**, IETE Journal of Research				
4.	Lakshmi Nediyara Suresh, Bhaskar Manickam	Design of Active Inductor-Based VCO with Wide Tuning Range for RF Front End	**Springer**, Circuits, Systems, and Signal Processing	41(5)	2486-2502	2021	2.311
5.	Lakshmi Nediyara Suresh, Bhaskar Manickam	Design and application of CMOS active inductor in bandpass filter and VCO for reconfigurable RF front-end	**Elsevier**, Integration, the VLSI Journal	82	115-126	2021	1.345
6.	S. Chrisben Gladson, P. Siva Prasad and M. Bhaskar	A 223-µW Single-to-Differential RF Mixer with 8.6dBm IIP3 using Current-Bleeding and Body-Effect for sub-6GHz 5G Applications	**Springer**, Analog Integrated Circuits and Signal Processing	109	571-583	2021	1.321
7.	S. Chrisben Gladson, P. Siva Prasad, V. Thenmozhi and M. Bhaskar	A 4-6 GHz Single-Ended to Differential-Ended Low-Noise Amplifier for IEEE 802.11ax Wireless Applications with inherent Complementary Distortion Cancellation	World Scientific, Journal of Circuits, Systems and Computers,	30	14(2150265)	2021	1.333
8.	S. Chrisben Gladson, Adith Hari Narayana · V, Thenmozhi, M. Bhaskar	A 219‑µW ultra‑low power low‑noise amplifier for IEEE 802.15.n4 based battery powered, portable, wearable IoT applications	Springer, **SN Applied Sciences**	3(4)	1-18	2021	2.11
9.	Arunkumar K.R. and Bhaskar M	Robust De-noising Technique for Accurate Heart Rate Estimation Using Wrist-type PPG Signals	**IEEE, Sensor Journal**	20	7980-7987	2020	4.325
10.	Chrisben Gladson S , M. Bhaskar,	A low-power RF mixer with harmonic cancellation for IEEE 802.15.4 portable, wearable wireless applications	**Elsevier**, International Journal of Electronics and Communications (AEÜ)	124	153335	2020	3.169
11.	S. Chrisben Gladson, M. Bhaskar	A 3-stage RF down-converter exploiting body-effect for IEEE 802.15.4 applications	**Elsevier**, Computers and Electrical Engineering	84	106615	2020	4.152
12.	Arunkumar, K.R., and Bhaskar, M	Combination of adaptive filters using single noise reference signal for heart rate estimation from PPG signals.	**Springer**, Signal, Image and Video Processing	14	1507-1515	2020	1.583
13.	Archana S and Bhaskar M	An Inductorless 1.8 mW 2.9dB NF Differential LNA Integrated to On-Chip Loop Antenna with Secondary Loop for Biomedical Applications	**Elsevier**, Microelectronics Journal	97	1-10	2020	1.992
14.	Lakshmaiah Alluri, Bhaskar M	Hemant Jeevan Magadum, Performance Assessment of RISC-V Architecture	International Journal of Recent Technology and	8	4576-4581	2020	0.675

			Engineering **(IJRTE)**				
15.	Lakshmi N S, Bhaskar Manickam	Multiple cascode flipped active inductor based tunable bandpass filter for fully integrated RF front-end	**IET** Circuits, Devices and Systems	**14**	**93-99**	**2020**	**1.297**
16.	Arunkumar K R, Bhaskar M	Heart rate estimation from wrist-type photoplethysmography signals during physical exercise	**Elsevier**, Biomedical Signal Processing and Control	**57**	**1-9**	**2019**	**5.076**
17.	S. Chrisben Gladson, M. Bhaskar	A 3-stage RF Down-Converter Network for IEEE 802.15.4 Applications	**Springer**, SN Applied Sciences	**61**	**1-17**	**2019**	**2.11**
18.	S. Chrisben Gladson, Adith Hari Narayana, M. Bhaskar	An ultra-low-power low-noise amplifier using cross-coupled positive feedback for 5G IoT applications	**Springer**, SN Applied Sciences	**1418**	**1-15**	**2019**	**2.11**
19.	S. Chrisben Gladson, R. Praveen, M. Bhaskar	A 0.1–2.75 GHz high-linear low-noise transconductance amplifier for high-performance multi-standard wireless applications	**Springer**, Microsystem Technologies	**26**	**2279-2295**	**2019**	**2.012**
20.	S. Chrisben Gladson, S. Vijayalakshmi, M. Sowmya Lakshmi, M. Bhaskar	Linearity improvement of RF mixer using double-linearization for 5 GHz applications	**Elsevier**, International Journal of Electronics and Communications (AEÜ)	**110**	**152856(1-14)**	**2019**	**3.169**
21.	Archana Sunitha, Bhaskar Manickam	Design and integration of a high gain low NF CG-Folded cascode inductor less balun-LNA with loaded on-chip loop antenna	**Elsevier**, International Journal of Electronics and Communications (AEÜ)	**110**	**152858(1-9)**	**2019**	**3.169**
22.	S. Chrisben Gladson, K. Alekhya, M. Bhaskar	A fully CMOS RF down-converter with 81.88 dB SFDR for IEEE 802.15.4 based wireless systems	**Springer**, Microsystem Technologies	**28**	**745-760**	**2019**	**2.012**
23.	S. Chrisben Gladson, M. Bhaskar, R. Praveen, S. Sudharsan	A 261-µW ultra-low power RF Mixer with 26-dBm IIP3 using complementary pre-distortion technique for IEEE 802.15.4 applications	**Elsevier**, International Journal of Electronics and Communication (AEÜ)	**107**	**70-82**	**2019**	**3.169**
24.	Archana Sunitha, Bhaskar Manickam	Co-design of on-chip loop antenna and differential class-E power amplifier at 2.4 GHz for biotelemetry applications	**Elsevier**, Microelectronics	**86**	**40-48**	**2019**	**1.992**
25.	Arunkumar K R, Bhaskar M	Heart rate estimation from photoplethysmography signal for wearable health monitoring devices	**Elsevier**, Biomedical Signal Processing and Control	**50**	**1-9**	**2019**	**5.076**
26.	S. Chrisben Gladson, M.	A low power high-performance area efficient RF	**Elsevier**, International	**96**	**81-92**	**2018**	**3.169**

	Bhaskar	front-end exploiting body effect for 2.4 GHz IEEE 802.15.4 applications	Journal of Electronics and Communications (AEÜ)				
27.	M. Bhaskar, Srinivas Gantasala, B. Venkataramani	Bidirectional differential on-chip wave-pipelined serial interconnect with surfing	**Springer**, Micro System Technologies	22	2611-2621	2015	2.012
28.	M.Bhaskar and B.Venkataramani	Differential Voltage Mode On-Chip Serial Transceiver for Global Interconnects, Journal of Low Power Electronics, American Scientific Publishers	Interconnects, Journal of Low Power Electronics, American Scientific Publishers	10	247-258	2014	0.4
29.	Bhaskar. M, Srinivas Gantasala, Venkataramani. B	Dynamic Self controllable surfing for differential on-chip wave pipeline serial interconnect	WSEAS Transactions on Circuits and Systems	13	117-128	2014	-
30.	Bhaskar. M and Venkataramani	Transceiver for Differential Wave Pipe-Lined Serial Interconnect with Surfing	International Journal of Electrical, Electronic Science and Engineering	8	155-162	2014	0.91
31.	Bhaskar. M, Jaswanth. A and Venkataramani	Design of a Novel Differential on-chip Wave-pipelined Serial interconnect with surfing	**Elsevier**, Microprocessor and Microsystems	37	649-660	2013	3.503

b) Conferences/Workshops/Symposia Proceedings
1) International Conferences

S. No.	Author(s)	Title of Abstract/ Paper	Title of the Proceedings	Venue	Year
1.	Debdas Paik, S Maheswari, Dr. Bhaskar M, M R Raghavendra	Implementation of Wide band Satellite Telemetry Data Receiver using SDR and Matlab	2nd Asian Conference on Innovation in Technology (ASIANCON)	Pune, India. Aug 26-28	2022
2.	Payavula Swathi, Bhaskar Manickam	A PVT invariant cascode current reference circuit in 180nm CMOS process	IEEE International Conference on Semiconductor Electronics(ICSE 2022)	Kuala Lampur Malaysia (Virtual)	2022
3.	Krishna Sai Tarun R, Ajith Kumar Reddy N,Pavan Kalyan C, Bhaskar M	Design and FPGA Implementation of High-Speed Area and Power Efficient 64-Bit Modified Dual CLCG Based Pseudo Random Bit Generator	7th IEEE International Symposium on Smart Electronic Systems	MNIT, Jaipur	2021

4.	V.Thenmozhi, M. Bhaskar	A high linear LC cross-coupled Low Noise Amplifier for X band applications	10th International Conference on Computing, Communication, and Sensor Networks	Kolkata, CCSN 2021	**2021**
5.	Aditya Sankaran, Srikanth Reddy Mummadi Arunkumar K R, Bhaskar Manickam	Design and Implementation of 1024 Point Pipelined Radix 4 FFT Processor on FPGA for Biomedical Signal Processing Applications	6th IEEE International Symposium on Smart Electronic Systems (iSES),	VIT, Chennai	**2020**
6.	Purushothaman, P, Alex Noel Josephraj , Srihari S and Bhaskar M	Hardware Implementation of Pyramidal Histogram of Oriented Gradients,	Academia Industry Consortium for Data Science	Wenzhou Kean University, Wenzhou, China	**2020**
7.	Lakshmaiah Alluri, M Bhaskar, Hemant Jeevan Magadum	Design of a smart controller for the self-learning of Differently Abled	IEEE-HYDCON	Hyderabad, India	**2020**
8.	S. Chrisben Gladson, V. Thenmozhi, M. Bhaskar	Design of 4-6 GHz Wideband Single-Ended to Differential-Ended LNA for IEEE 802.11ax Wireless Applications	7th International Conference on Microelectronics, Circuits & Systems	Kolkata,	2020
9.	S Chrisben Gldson, V. Thenmozhi and Bhaskar M	A 624μW Variable gain amplifier with 45dB peak gain using current controlled degeneration	IEEE 5th International conference on Devices Circuits and Systems (ICDCS 2020)	Karunya University, Coimbatore,	**2020**
10.	Archana S, Bhaskar M	An LTCC based H-Antenna Aperture Coupled to an On-Chip Antenna for 2.4 GHz Long Range Transmitters	Electronic Packaging and Technology Conference (EPTC 2019)	Singapore	**2019**
11.	J. Pradeep, S. Chrisben Gladson, M. Bhaskar	A low power wideband low-noise amplifier with input series peaking and gm enhancement for 0.5 – 3.5 GHz applications	IEEE TENCON 2019,	Kochi	**2019**
12.	S. Chrisben Gladson, Nitin Kumar, M. Bhaskar	Study of the Effect of Pseudo-Sine Wave as a LO on the Linearity Performance of the RF Mixer	IEEE International Conference on Vision Towards Emerging Trends in Communication And Networking	VIT, Vellore	**2019**
13.	Archana S and Bhaskar M	A meandered loop antenna-in package with parasitic structure at 2.4 GHz	IEEE Electrical Design of Advanced Packaging and Systems	Chandigarh, India	**2018**

			Symposium (EDAPS),		
14.	S. Chrisben Gladson, R. Praveen, M. Bhaskar	Wideband High Linear Low-Noise Transconductance Amplifier for High-Performance Wireless Applications	7th International Conference on Computing, Communication, and Sensor Networks	Kolkata	**2018**
15.	Arunkumar K R , Ram Srivathsa and Bhaskar M	Improved Heart Rate Estimation from Photoplethysmography During Physical Exercise Using Combination of NLMS and RLS Adaptive Filters	IEEE Region 10 Conference (TENCON)	Jeju Island, South Korea	**2018**
16.	Lakshmi N S, Bhaskar M	Gyrator-C Based Bandpass Filter with Improved Dynamic Range for Fully Integrated RF Front-end	IEEE Computer Society Annual Symposium on VLSI	ISVLSI, Hong Kong	**2018**
17.	S. Chrisben Gladson, K. Alekhya, M. Bhaskar	An LNTA based Mixer with Post-Distortion Harmonic Cancellation for 2.4GHz IEEE 802.15.4 Applications	5th International Conference on Microelectronics, Circuits and Systems	Bhubaneswar	**2018**
18.	S. Chrisben Gladson, K. Alekhya, M. Bhaskar	Low-Power High Linear RF Mixer for 2.4GHz Low-Rate WPAN Applications	4th IEEE International Conference on Circuits, Devices, and Systems	Coimbatore	**2018**
19.	S. Chrisben Gladson, M. Bhaskar	A Fully CMOS Inductor-less Folded Cascode Double-Balanced Mixer with High Conversion Gain for 2.4GHz WPAN Applications	1st International Conference on Recent Innovations in Electrical, Electronics, and Communication Systems	Dehra Dun	**2017**
20.	R Thilagavathy, Susmitha Settivari, B Venkataramani, M Bhaskar	FPGA Implementation of a Novel Area Efficient FFT Scheme Using Mixed Radix FFT	International Symposium on VLSI Design and Test, VDAT 2017	Roorkee	**2017**
21.	Reishi Kumar, Anamika Sharma, M.Bhaskar	Reference table-based cache design using LRU replacement algorithm for Last Level Cache	IEEE, TENCON 2016	Singapore	**2016**
22.	Srivignessh Pss and Bhaskar. M,	RFID and Pose Invariant Face Verification Based Automated Classroom Attendance System	IEEE, Microcom	NIT, Durgapur	**2016**
23.	Bhaskar.M, Srinivas Gantasala and B. Venkataramani,	Dynamic Self controllable Surfing for Differential on-chip wave-pipelined serial interconnect	1st International conference on Microelectronics, Circuits and Systems (MICRO-	Kolkata	**2014**

				2014)		
24.	Bhaskar.M, Prasannakumar.D and Venkataramani.B	Design of Differential voltage mode Transmitter for On-chip serial link based on Method of Logical Effort	IEEE-ICCCNT	Coimbatore	**2012**
25.	M.Bhaskar, D.Sridevi and B.Venkataramani	A Low Power, Low Latency Tunable Quasi- Resonant Interconnect using Active Inductor	IEEE-RAICS, Recent Advances in Intelligent Computational Systems	Trivandrum	**2011**
26.	M.Bhaskar, D.Parthiban and B.Venkataramani,	Design and Implementation of Surfing scheme to Wave pipelined Differential serial Interconnect,	IEEE-RAICS, Recent Advances in Intelligent Computational Systems	Trivandrum	**2011**
27.	V.Mohana Vidya, R.Thilagavathy and M.Bhaskar,	Low Power, High Performance Current mode Transceiver for Network-on-Chip Communication	IEEE-ICSCCN 2011	Noorul Islam Centre for Higher Education, Nagarcoil	**2011**
28.	Karutharaja.V, M.Bhaskar and B.Venkataramani	Synchronization of On-chip Serial Interconnect transceivers using Delay Locked Loop (DLL)	IEEE- ICSCCN 2011, International conference on Signal Processing, Communication, Computing and Networking Technologies	Noorul Islam Centre for Higher Education, Nagarcoil	**2011**
29.	M.Bhaskar, B.Venkataramani and G.Praveen	Implementation of Asynchronous Transceivers for on-chip Interconnects using Self-clocked Circuits in 0.18 µm	ICRAES 2010, International Conference on Recent Advances in Electrical Sciences	K.S.R. College of Engineering Tiruchengo de	**2010**
30.	J Manikandan, B Venkataramani, M Bhaskar, K Ashish, R Raghul, V Mathangi,	Implementation of a novel phoneme recognition system using TMS320C6713 DSP	23rd International Conference on VLSI Design	Bangalore, India	**2010**
31.	Venkateswaralu, M.Bhaskar and B.Venkataramani	Quasi-resonant Interconnects: Programmable data rate implementation using Active Inductor	ICOICT 2009, International conference sponsored by TEQIP	Trivandrum	**2009**
32.	Kirankumar, M.Bhaskar, R.Thilagavathy and B.Venkataramani	A Novel Low power multilevel current mode Interconnect system ineffective to supply voltage variations	ICOICT 2009, International conference sponsored by TEQIP	Trivandrum	**2009**

| 33. | P.Murugeswari, G.Anusha, P.Venkateshwarlu, M.Bhaskar and B.Venkataramani | A Wide band voltage mode sense amplifier receiver for high speed Interconnects, | TENCON 2008 | Hydrabad | **2008** |
| 34. | G.Anusha, P.Venkateshwarlu, P.Murugeshwari, M.Bhaskar and B.Venkataramani, | An Input Multiplexed current mode Transmitter for on-chip global Interconnects | TENCON 2008 | Hydrabad | **2008** |

2) National Conferences

S. No.	Author(s)	Title of Abstract/ Paper	Title of the Proceedings	Venue	Year
1.	Archana Sunitha, Bhaskar M	A 2.4 GHz High Efficiency Capacitive Cross Coupled Common Gate Class-E Differential Power Amplifier	23rd International Symposium on VLSI Design and Test (VDAT 2019)	Indore	**2019**
2.	M.Bhaskar, D.Parthiban and B.Venkataramani	Design and Implementation of Differential serial interconnect using Wavepipelining and Surfing	VDAT 2011, 15th VLSI Design and Test Symposium at Wipro Technologies	Pune	**2011**
3.	Karutharaja.V, M.Bhaskar and B.Venkataramani	Implementation of High-speed Delay Locked Loop (DLL) for On-chip Serial Interconnect transceivers	National conference on Advancements and Future trends in VLSI Design	Kalasalingam University, Virudhunagar	**2011**
4.	K.Venkatesh Reddy, M.Bhaskar and B.Venkataramani	Implementation of Multi-phase Delay Locked Loop for On-Chip serial link, NCSCV 2010	2nd National Conference on Signal Processing Communications & VLSI Design	Anna University, Coimbatore	**2010**
5.	T.Gvardhana rao, M.Bhaskar and B.Venkataramani	Differential voltage mode Sense amplifier with Current mirror load as receiver for on-chip Interconnect Serial links	NCSCV 2010, 2nd National Conference on Signal Processing Communications & VLSI Design	Anna University, Coimbatore	**2010**
6.	Nitin Bhomle , M. Bhaskar and B.Venkatramani	An Input Multiplexed Current mode Transmitter with Modified driver for on-chip serial Interconnect system	NCSCV 2010, 2nd National Conference on Signal Processing Communications & VLSI Design	Anna University, Coimbatore	**2010**
7.	M. Sharath Bimba, M. Bhaskar and B. Venkataramani	Implementation of Active Inductor for Quasi-Resonant Interconnect	NCVESCOM 2010, 3rd National Conference on VLSI, Embedded Systems, Signal Processing and Communication Technologies	Vinayaka Mission University, Chennai	**2010**

c) Books & Monographs

Author(s)	Title of Book/Monograph	Name of Publishers	Year of Publication	ISSN/ISBN Number
M. Bhaskar and B. Venkataramani	'Digital Signal Processors, Architecture, Programming and Applications	Tata McGraw Hill, New Delhi	1st Edition: 2002 2nd Edition: 2010	ISBN(13): 978-0-07-070256-1 ISBN(10):0-07-070256-X