Government of India
Ministry of Human Resource Development

GIAN

GLOBAL INITIATIVE OF ACADEMIC NETWORKS

MAY 9th- 13th, 2022
DEEP LEARNING PROCESSOR ARCHITECTURE
(ONLINE MODE)

Overview

Deep Neural Networks (DNNs) are widely used for many AI applications including computer vision, speech recognition, robotics, etc. While DNNs deliver state-of-the-art accuracy on many AI tasks, it comes at the cost of high computational complexity. Accordingly, designing efficient hardware architectures for deep neural networks is an important step towards enabling the wide deployment of DNNs in AI systems. Deep learning consists of deep networks of varying topologies. Neural networks have been around for quite a while, but the development of numerous layers of networks made them more practical to use. Adding layers means more interconnections and weights between and within the layers. This is where GPUs benefit deep learning, making it possible to train and execute these deep networks (where conventional processors are not as efficient). A deep learning accelerator core providing high compute efficiency and utilization will be discussed which can achieve performance and area efficiency. This core can be a practical building block for System on Chip (SOC) to enable a broad range of AI hardware systems.

Course participants will learn various pertaining topics through lectures and hands-on experiments. Also, case studies showing Industrial/research use and assignments will be shared to stimulate research motivation of participants.

Modules	**Deep Learning Overview:** **May 9th, 2022** **Deep Learning Processor – FPGA:** **May 10th,2022** **Deep Learning Processor – ASIC:** **May 11th,2022** **Deep Learning Hardware - Software Co-Design:** **May 12th,2022** **Deep Learning Processor Evaluation and Summary:** **May 13th,2022** **The number of participants for the course will be limited to FIFTY**
You Should Attend If…	• You are an electronics engineer, or research scientist interested in designing deep learning processor architecture for image exploration. • You are a professional engineer willing to enhance the knowledge, on hardware and software co-design for deep learning processor. • You are a student or faculty from an academic institution interested in learning how to implement deep learning processor architecture on FPGA and ASIC.
Fees	The participation fees for taking the course is as follows: **Participants from Abroad:** **US $500** **Industry/ Research Organizations:** **Rs. 7,000/-** **Academic Institutions Faculty:** **Rs. 2,000/-** **Students and Research Scholars:** **Rs. 1,000/-**

The faculty

Seok-Bum Ko is currently a Professor and Head at the Department of Electrical and Computer Engineering and the Division of Biomedical Engineering, University of Saskatchewan, Canada.
He got his PhD degree from the University of Rhode Island, USA in 2002. His research interests include computer architecture/arithmetic, efficient hardware implementation of compute-intensive applications, deep learning processor architecture and bio medical engineering. He is a senior member of IEEE circuits and systems society and associate editor of IEEE TVLSI, IEEE Access and IEEE TCASI (2020-2021).

Dr. S. Deivalakshmi is currently an Assistant Professor of Department of Electronics and Communication Engineering, National Institute of Technology, Tiruchirappalli, India. Her research interests include Artificial Intelligence, Signal and Image Processing.

Dr. R. Pandeeswari is currently an Associate Professor in the Department of Electronics and Communication Engineering, National Institute of Technology, Tiruchirappalli. Her research interests include Metamaterial Inspired Antennas, Deep learning techniques for 5G antennas.

Course Coordinators

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