National Institute of Technology, Tiruchirappalli:
Performa for CV of Faculty/ Staff Members

Curriculum Vitae

B. Naresh Kumar Reddy is an assistant professor at the Department of Electronics and Communication Engineering, National Institute of Technology Tiruchirappalli, and is currently involved in various teaching/research-related areas like FPGA Architectures, VLSI and Embedded Systems, Networks-on-Chip, Design methodologies for System-on-Chip, Reconfigurable Architectures. He has published in more than 15 SCI journals and 20 IEEE conferences. He is a senior member of the IEEE and a member of ACM.

Google Scholar ID: https://scholar.google.co.in/citations?user=HSqqGF4AAAAJ&hl=en

Scopus ID: https://www.scopus.com/authid/detail.uri?authorId=57802544300

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DBLP: https://dblp.org/pid/140/8798.html

1. Name: B. Naresh Kumar Reddy
2. Designation: Assistant Professor
3. Office Address: Department of ECE, NITT
4. Telephone (Direct) (Optional):

   Telephone : Extn (Optional):

   Mobile (Optional): 9966539090
5. Email (Primary): bnkreddy@nitt.edu Email (Secondary): naresh.nitg@gmail.com
6. Field(s) of Specialization: MPSoC, Network-on-Chip, Embedded System and VLSI.
7. Employment Profile

Job Title	Employer	From	To
Assistant Professor	Indian Institute of Information Technology and Management-Kerala	2021	2022
Post-Doctoral Fellow	Indian Institute of Technology Delhi	2020	2021
Assistant Professor	IFHE, ICFAI University	2018	2020

8. Academic Qualifications (From Highest Degree to High School):

Examination	Board / University	Year	Division/ Grade	Subjects
Ph.D (E.C.E)	National Institute of Technology Goa	2018	--	Multi-Processor System-on-Chip
M.Tech (Embedded Systems)	K.L.University	2012	Distinction	Embedded Systems
B.Tech (E.C.E)	S.V.University	2010	First Class	Electronics and Communication Engineering
HSC (Intermediate/ +2)	Nalanda Junior College, Kadapa.	2006	A Grade	Maths, Physics, and Chemistry
SSC (10th)	Parameswara High School	2004	First Class	SSC

9. Academic/Administrative Responsibilities within the University

Position	Faculty/Department/Centre/Institution	From	To

10. Academic/Administrative Responsibilities outside the University

Position	Institution	From	To

11. Awards, Associateships etc.

Year of Award	Name of the Award	Awarding Organization

12. Fellowships

Year of Award	Name of the Fellowship	Awarding Organization	From (Month/Year)	To (Month/Year)
2015	Visvesvaraya PhD Scheme	MeitY	01/2015	12/2017

13. Details of Academic Work

(i) Curriculum Development

(ii) Courses taught at Postgraduate and Undergraduate levels

UG Level:

1. Digital Circuit & Systems
2. Microprocessor and Microcontrollers
3. Embedded Systems
4. Computer Architecture & Organization
5. ARM System architecture
6. Digital VLSI Testing

PG Level:

1. Modelling & Synthesis with Verilog HDL
2. Functional Verification using Hardware Verification Language
3. Embedded System Design
4. FPGA based System Design

(iii)Projects guided at Postgraduate level

(iv)Other contribution(s)

14. Details of Major R&D Projects

Title of Project	Funding Agency	Duration		Status
		From	To	Ongoing/ Completed

15. Number of PhDs guided

Name of the PhD Scholar	Title of PhD Thesis	Role(Supervisor/ Co-Supervisor)	Year of Award

16. Participation in Workshops/ Symposia/ Conferences/ Colloquia /Seminars/ Schools etc. (mentioning the role)

Date (s)	Title of Activity	Level of Event (International/ National/ Local)	Role (Participant/ Speaker/ Chairperson, Paper presenter, Any other)	Event Organized by	Venue
07th Aug 2020	International Symposium on, "Energy and Sustainable Development: A Gandhian Approach"	International	Participant	IIT Patna and Aalborg University, Denmark	IIT Patna

17. Workshops/ Symposia/ Conferences/ Colloquia/Seminars Organized (as Chairman/ Organizing Secretary/ Convenor / Co-Convenor)

Title of Activity	Level of Event (International/ National/ Local)	Date (s)	Role	Venue

18. Invited Talks delivered

Topic	Date	Inviting Organization

19. Membership of Learned Societies

Type of Membership (Ordinary Member/ Honorary Member / Life Member)	Organization	Membership No. with date
Senior Member	IEEE	93668441
Member	ACM	5553133
Life Member	International Association of Engineers	144416

20. Academic Foreign Visits

Country	Duration of Visit	Programme

21. Publications

(A) Refereed Research Journals:

1. **B. Naresh Kumar Reddy**, and Subrat Kar, "Performance evaluation of modified mesh-based NoC architecture," Computers and Electrical Engineering, Volume 104, Part A, 2022. (Impact Factor= **4.152**)
   https://doi.org/10.1016/j.compeleceng.2022.108404

2. **B. Naresh Kumar Reddy**, B Seetharamulu, GS Krishna, BV Vani, "An FPGA and ASIC Implementation of Cubing Architecture," Wireless Personal Communications, Vol. 125, pp. 3379-3391, 2022. (Impact Factor= **2.017**)
   https://doi.org/10.1007/s11277-022-09715-w

3. **B. Naresh Kumar Reddy** "Design and implementation of high performance and area efficient square architecture using Vedic Mathematics," Analog Integrated Circuits and Signal Processing, Vol. 102, pp. 501–506, 2020. (Impact Factor= **1.337**) – **Single Author**
https://doi.org/10.1007/s10470-019-01496-w

4. **B. Naresh Kumar Reddy**, BV Vani, GB Lahari "An efficient design and implementation of Vedic multiplier in quantum-dot cellular automata," Telecommunication Systems, Vol. 74, pp. 487–496, 2020. (Impact Factor= **2.336**)
https://doi.org/10.1007/s11235-020-00669-7

5. **B. Naresh Kumar Reddy**, Vasantha.M.H. and Nithin Kumar Y.B., "An Energy Efficient Fault-Aware Core Mapping in Mesh-based Network on Chip Systems," Journal of Network and Computer Applications, Vol. 105, pp. 79-87, 2018. (Impact Factor= **7.574**)
https://doi.org/10.1016/j.jnca.2017.12.019

6. **B. Naresh Kumar Reddy**, Vasantha.M.H. and Nithin Kumar Y.B., "Hardware Implementation of Fault Tolerance NoC Core Mapping," Telecommunication Systems (TELS), Vol 68, pp. 621- 630, 2018. (Impact Factor= **2.336**)
https://doi.org/10.1007/s11235-017-0412-2

7. **B. Naresh Kumar Reddy**, Vasantha.M.H. and Nithin Kumar Y.B., "Energy- Aware and Reliability- Aware Mapping for NoC-Based Architectures," Wireless Personal Communications, Vol. 100, pp. 213- 225, 2018. (Impact Factor= **2.017**)
https://doi.org/10.1007/s11277-017-5061-y

8. **B. Naresh Kumar Reddy**, Vasantha.M.H., and Nithin Kumar Y.B., "System Level Fault-Tolerance Core Mapping and FPGA-based Verification of NoC," Microelectronics Journal, Vol. 70, pp. 16- 26, 2018. (Impact Factor= **1.992**)
https://doi.org/10.1016/j.mejo.2017.09.010

9. **B. Naresh Kumar Reddy**, Vasantha.M.H., and Nithin Kumar Y.B., "High-Performance and Energy-Efficient Fault-Tolerance Core Mapping in NoC," Sustainable Computing, Informatics and Systems, Vol. 16, pp. 1- 10, 2018. (Impact Factor= **4.923**)
https://doi.org/10.1016/j.suscom.2017.08.004

10. **B. Naresh Kumar Reddy**, C Ramalingaswamy, R Nagulapalli, D Ramesh "A novel 8T SRAM with improved cell density," Analog Integrated Circuits and Signal Processing, Vol. 98, Issue 2, pp. 357-366, 2019. (Impact Factor= **1.321**)
https://doi.org/10.1007/s10470-018-1309-z

11. **B. Naresh Kumar Reddy**, Dharavath Kishan, and B. Veena Vani, "Performance constrained multi-application network on chip core mapping," International Journal of Speech Technology, Vol 22, pp.927-936, 2019.
https://doi.org/10.1007/s10772-019-09636-3

12. A. Sai Kumar and **B. Naresh Kumar Reddy**, "An Efficient Real-Time Embedded Application Mapping for NoC Based Multiprocessor System on Chip," Wireless Personal Communications, 2022. (Impact Factor= **2.017**)
https://doi.org/10.1007/s11277-022-10080-x

13. A. Sai Kumar, TVK H Rao and **B. Naresh Kumar Reddy**, "Performance and communication energy constrained embedded benchmark for fault tolerant core mapping onto NoC architectures," International Journal of Ad Hoc and Ubiquitous Computing, Vol 41, pp. 108-117, 2022. (Impact Factor= **0.773**)
https://doi.org/10.1504/IJAHUC.2022.125427

14. K. Raghava Rao, Md Zia Ur Rahman, Krishna Prasad Satamraju and **B Naresh Kumar Reddy**, "Genetic Algorithm for Cross-Layer based Energy Hole Minimization in Wireless Sensor Networks," IEEE Sensors Letters, 2022. (Impact Factor= **3.04)**
https://doi.org/10.1109/LSENS.2022.3219857

15. Pittala, C.S., Vijay, V. and **B. Naresh Kumar Reddy**, "1-Bit FinFET Carry Cells for Low Voltage High-Speed Digital Signal Processing Applications," Silicon (2022). (Impact Factor= **2.941**)
https://doi.org/10.1007/s12633-022-02016-8

16. Javvaji, V., Musala, S. and **B. Naresh Kumar Reddy**, "Continuous-time complex band-pass Gm-C sigma delta ADC with programmable bandwidths," Analog Integrated Circuits and Signal Processing, Vol. 108, pp. 267–276, 2021. (Impact Factor= **1.337**)
https://doi.org/10.1007/s10470-021-01866-3

17. Ahmed, S., Ramesh, N.V.K. and **B. Naresh Kumar Reddy,** "A Highly Secured QoS Aware Routing Algorithm for Software Defined Vehicle Ad-Hoc Networks Using Optimal Trust Management Scheme," Wireless Personal Communications, Vol. 113, pp. 1807–1821, 2020. (Impact Factor= **2.017**)
https://doi.org/10.1007/s11277-020-07293-3

18. Yehoshuva, C., **B. Naresh Kumar Reddy**., Ambati, V.R., "A novel CMOS Gmm-C complex filter design for multi-mode multi band wireless receiver applications," Analog Integrated Circuits and Signal Processing, Vol. 91, pp. 43–51, 2017. (Impact Factor= **1.321**)
https://doi.org/10.1007/s10470-016-0823-0

(B) Conferences/Workshops/Symposia Proceedings

1. **B Naresh Kumar Reddy**, Alex James and Sai Kumar, "Fault-tolerant Core Mapping for NoC Based Architectures with Improved Performance and Energy Efficiency," 29th International Conference on Electronics, Circuits, and Systems (ICECS-2022), **Glasgow, UK, Oct 24-26, 2022.**

2. **B Naresh Kumar Reddy** and Subrat Kar "An Efficient Application Core Mapping Algorithm for Wireless Network-on-Chip," 26th IEEE Pacific Rim International Symposium on Dependable Computing (PRDC 2021), Dec 1– 4, in **Perth, Australia**, 2021.
https://doi.org/10.1109/PRDC53464.2021.00028

3. **B Naresh Kumar Reddy** and Subrat Kar "Energy Efficient and High Performance Modified Mesh Based 2-D NoC Architecture," 22nd IEEE International Conference on High Performance Switching and Routing (HPSR), June 7 – 9, in **Paris, France**, 2021.
https://doi.org/10.1109/HPSR52026.2021.9481796

4. Sudheer H, G Sai Vishal Reddy and **B Naresh Kumar Reddy**, "Design and Analysis of High Reliable Fault Tolerance Subsystem for Micro Computer Systems," 11th IEEE Symposium on Computer Applications & Industrial Electronics (ISCAIE 2021), **Penang, Malaysia**, pp. 127-130, 2021.
https://doi.org/10.1109/ISCAIE51753.2021.9431830

5. Sai Kumar, T.V.K.Hanumatha Rao and **B. Naresh Kumar Reddy**, "Exact Formulas for Fault Aware Core Mapping on NoC Reliability," 17th International IEEE India Conference **INDICON**, 2020.
https://doi.org/10.1109/INDICON49873.2020.9342427

6. **B Naresh Kumar Reddy**, G Sai Vishal Reddy, B Veena Vani, "Design and Implementation of an Efficient LFSR using 2-PASCL and Reversible Logic Gates," IEEE Bombay Section Signature Conference (**IBSSC**), pp. 247-250, 2020.
https://doi.org/10.1109/IBSSC51096.2020.9332213

7. **B. Naresh Kumar Reddy**, Sarangam K, T. Veeraiah and Ramalingaswamy Cheruku "SRAM cell with better read and write stability with Minimum area," IEEE **TENCON** 2019.
https://doi.org/10.1109/TENCON.2019.8929593

8. **B. Naresh Kumar Reddy**, Vasantha.M.H. and Nithin Kumar Y.B., "An Efficient Core Mapping Algorithm on Network on Chip," 22nd International Symposium on VLSI Design and Test (**VDAT**), 2018.
https://doi.org/10.1007/978-981-13-5950-7_52

9. **B. Naresh Kumar Reddy**, Vasantha.M.H. and Nithin Kumar Y.B., "A Gracefully Degrading and Energy-Efficient Fault Tolerant NoC Using Spare core," 2016 IEEE Computer Society Annual Symposium on VLSI (**ISVLSI** 2016), **Pennsylvania, U.S.A**., pp. 146-151, 2016.
https://doi.org/10.1109/ISVLSI.2016.80

10. Vijaya Sree Boddu, **B. Naresh Kumar Reddy** and M. Kranthi Kumar, "Low-Power and Area Efficient N-bit Parallel Processors on a Chip," 13th International IEEE India Conference **INDICON** 2016, pp. 1-4, 2016. https://doi.org/10.1109/INDICON.2016.7839082

11. **B. Naresh Kumar Reddy**, Vasantha.M.H., Nithin Kumar Y.B. and Dheeraj Sharma, "Communication Energy Constrained Spare Core on NoC," 6th International Conference on Computing, Communication and Networking Technologies (ICCCNT), **Dallas, U.S.A**., pp. 1-4, 2015. https://doi.org/10.1109/ICCCNT.2015.7395168

12. **B. Naresh Kumar Reddy**, Vasantha.M.H., Nithin Kumar Y.B. and Dheeraj Sharma, "A Fine Grained Position for Modular Core on NoC," IEEE International Conference on Computer, Communication and Control, Sep 2015. https://doi.org/10.1109/IC4.2015.7375574

(C) Books & Monographs

Author(s)	Title of Book/Monograph	Name of Publishers	Year of Publication	ISSN/ISBN Number