**Curriculum Vitae**

**Dr.G.Lakshminarayanan**
Associate Professor, Department of Electronics & Communication Engineering,
National Institute of Technology, Tiruchirappalli, Tamil Nadu, India
Email: laksh@nitt.edu Mobile: +91 94429 40144 TP: +91-431-250 3307
Website:
http://www.nitt.edu/home/academics/departments/ece/faculty/associate_professor/gln/

**Dr.G.Lakshminarayanan** is an **Associate Professor** in the Department of Electronics and Communication Engineering at NIT-Trichy, India. His research interests are primarily in the areas of VLSI based Wireless System Design/Physical Layer Design, Algorithms and Techniques for Cognitive Radio, Design of Asynchronous Systems and Reconfigurable systems. He is carrying out research work on Design and implementation of High Performance Digital VLSI Architectures and FPGA based System Design. One patent has been granted to him and another one filed. R&D projects carried out by him includes the design and development of Wireless transceivers for Cognitive Radio, MB-OFDM UWB Wireless system, On-Chip Speech Recognition System and TIDE. ASIC Chip has been fabricated by him on 0.18 µm technology.

He carried out his research work leading to Ph.D. at National Institute of Technology, Tiruchirappalli under the guidance of Dr.B.Venkataramani, Professor (HAG), NIT, Trichy. During his Ph.D., he used FPGA as a platform to explore the possibilities of implementing wave pipelined circuits. He served in one of the VLSI design companies, SASKEN COMMUNICATION TECHNOLOGIES LIMITED, BANGALORE and was involved in the project "FPGA implementation of USB Sub System". His job was to do FPGA timing closure. He used Virtex-4 FPGA and successfully completed the job. He has been in the FPGA/ VLSI field from 1999.

1. Name — Dr.G.Lakshminarayanan
2. Designation: — Associate Professor
3. Office Address: — Administrative block, NIT-Trichy.
4. Telephone (Direct) (Optional): — 0431-2503307
   Telephone : Extn (Optional):
   Mobile (Optional): — +91-9442940144
5. Email (Primary): laksh@nitt.edu — Email (Secondary) :
6. Field(s) of Specialization: — VLSI based system design

7. Employment Profile

| Job Title | Employer | From | To |
|---|---|---|---|
| Scientist 'B' cum Research Associate | NIT-Trichy | Dec-2000 | Oct-2004 |
| Senior Design Engineer | Sasken Communication Technologies Ltd., Bangalore | Nov-2004 | Aug-2005 |
| Assistant Professor | Saranathan College of Engineering, Trichy | Sep - 2005 | Nov- 2006 |
| Assistant Professor | TIFAC CORE, Sastra University - Thanjavur | Dec -2006 | May - 2007 |
| Assistant Professor | NIT-Trichy | Jun- 2007 | May - 2010 |
| Associate Professor | NIT-Trichy | Jun – 2010 | Till date |

8. Academic Qualifications (From Highest Degree to High School):

| Examination | Board / University | Year | Division/ Grade | Subjects |
|---|---|---|---|---|
| Ph.D. | Bharathidasan University (Work carried out at NIT-Trichy) | 2005 | -- | VLSI Systems/ Electronics and Communication Engineering |
| M.E. | NIT-Trichy | 1995 | I | Communication Systems |
| A.M.I.E | The Institution of Engineers (I), Kolkatta | 1991 | -- | Electronics and Communication Engineering |
| Diploma | Department of Technical Education, Madras | 1987 | I | Electronics and Communication Engineering |
| S.S.L.C | Board of Secondary Education, Tamil Nadu | 1984 | I | |

9. Academic/Administrative Responsibilities within the University

| Position | Faculty/Department/Centre/ Institution | From | To |
|---|---|---|---|
| Maintenance in-charge | All seminar Halls | 2008 | 2012 |
| Class Coordinator | ECE Department | 2007 | 2015 |
| PAC Chairman | ECE Department | 2007 | Till Date |
| DPC Member | ECE Department | 2007 | Till Date |
| Project Coordinator – B.Tech. | ECE Department | 2014 | 2014 |
| TEQIP – Department Coordinator | Institute | 2011 | Till Date |
| DAC Member/ EEE Department | Institute | 2013 | Till Date |
| Ph.D./ M.S. - Entrance Exam Committee Member | ECE Department | 2010 | 2014 |
| Wireless and Communication Lab. In-charge | ECE Department | 2010 | Till Date |
| VLSI Lab. In-charge | ECE Department | 2007 | 2010 |
| Maintaining Imprest | ECE Department | 2008 | 2015 |
| Member:<br>1. Institute day<br>2. Convocation Day | Institute | 2008 | Till Date |
| Staff Advisor: Festember | Institute | For 2 years | |
| Member: First year Orientation Programme | Institute | 2013 | Till Date |
| Faculty Volunteer – The Hon'ble President of India visit | Institute | 19.07.2014 | |
| One of the Coordinators for establishing Wireless System Design Lab. | ECE Department | 2013 | Till Date |
| Member:<br>1. CECASE<br>2. CEESD<br>3. STG<br>4. E-Content | Institute | 2012 | Till Date |
| Member of Research Council | Institute | 2011 | Till Date |
| CEDI - One of the Directors | Institute | 2012 | Till Date |

10. Academic/Administrative Responsibilities outside the University

| Position | Institution/ Organization | From | To |
|---|---|---|---|
| ECE – BOS Member | PSG Tech., Coimbatore | 2012 | 2014 |
| ECE – BOS Member | CIT, Coimbatore | | |

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|---|---|---|---|
| ECE – BOS Member | Kongu Engineering College, Preundurai, Eroad | 2010 | |
| ECE – BOS Member | Periyar Maniammai University, Tanjavur | | |
| ECE – BOS Member | Periyar Centenary Polytechnic College, Tanjavur | | |
| First time Collaborator | SAMEER-CEM, Chennai | 2010 | 2011 |
| First time Collaborator | CDAC, Trivandrum | 2010 | Till Date |

**In addition –**

1. **Doctoral Committee Member for almost all the Deemed Universities like VIT, Vellore, Vignan Unversity, Hyderabad**
2. **Examiner for Ph.D. Scholars including Anna University, Chennai**
3. **Reviewer for Journals including IEEE, IET**

11. Awards, Associateships etc.

| Year of Award | Name of the Award | Awarding Organization |
|---|---|---|
| 1995 | Second Rank in M.E. (IV/V Sem) | NIT Trichy |
| 2012 | UKIERI Project Awardee | British Council |
| May 15, 2008 | **Patent Title:** Improved wave pipelined array multiplier | Indian Patent Office (No. 220117) |
| March 01, 2013 | **Patent Title:** Design of Global Asynchronous Controller | Indian Patent Office (Application Number: 596/CHE/2013) |

12. Fellowships

| Year of Award | Name of the Fellowship | Awarding Organization | From (Month/Year) | To (Month/Year) |
|---|---|---|---|---|
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13. Details of Academic Work

(i) Curriculum Development:
Revising/ updating the syllabus of the courses taught by me every year at both UG & PG levels

(ii) Courses taught at Postgraduate and Undergraduate levels:

PG Level:

1. EC654 EDA tools
2. EC661 Digital System Design
3. EC662 Modeling and Synthesis with Verilog HDL

4. EC803 Optimizations of DSP Structures for VLSI
5. EC656 Design of ASICs
6. EC664 Cognitive Radio
7. EC666 Analysis and Design of Digital Systems using AHDL
8. EC669 VLSI DSP Systems
9. EC670 Asynchronous System Design

UG Level:

1. ECPC21 Analog Communication
2. ECPC14 Digital Circuits and Systems

(iii)Projects guided at Postgraduate level:

Guiding 5 students of M.Tech. (VLSI System) every semester from 2007

(iv)Other contribution(s):

1. Involvement in Laboratory development:
   Coordinated in developing the following labs.:
   1. VLSI Design Lab.
   2. Wireless Communication Lab.
   3. Wireless System Design Lab. under FIST fund
2. Involvement in development of Experiments in the laboratory:
   Experiments in-all developed for the Laboratories given below:
   1. HDL Programming Lab. – Total of 12 experiments developed by me
   2. ASIC-CAD Lab. – With various EDA tools, Total of 12 experiments developed by me
3. Received 25 numbers of "Xilinx ISE Design Suit: System" edition Licenses and 3 numbers of "Partial Reconfiguration Licenses" worth Rs.3,76,000 on June 2012 from Xilinx Inc for Free of Cost.
4. Received the following VLSI Tools free of cost- Xilinx ISE Software (every now and then updated) worth Rs. 2 lakh, Xilinx Hardware boards worth Rs. 2 lakh and Altera Hardware board worth Rs. 0.5 lakh during 2005 -06
5. Guiding 3 batches of students at UG level every year from 2007

14. Details of Major R&D Projects

| Title of Project | Funding Agency | Duration | | Status |
|---|---|---|---|---|
| | | From | To | Ongoing/ Completed |
| Design and Implementation of MB-OFDM UWB Transceiver Modules using Asynchronous Pipelining | DeitY, New Delhi | Feb 2008 | Feb 2011 | Completed |

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|---|---|---|---|---|
| "Special Manpower Development programme for VLSI (SMDP-II) | DeitY, New Delhi | Feb 2006 | Feb 2012 | Completed |
| Low complexity Energy efficient Transceivers for Cognitive Radio System | UKIERI - Department of S&T, New Delhi | Feb 2012 | Feb 2014 | Completed |
| Rural and Remote Ubiquitous Broadband Wireless Access | UKIERI - Department of S&T, New Delhi | Feb 2012 | Feb 2014 | Completed |
| Setting up Wireless System Design Lab. | Department of S&T, New Delhi | 2012 | 2017 | On going |
| Low complexity Energy efficient Transceivers for OFDM based Cognitive Radio | DeitY, New Delhi | | | Approval Obtained, Fund yet to be received. |
| C2SD – SMDP III - Carrying out Cluster Project with IITM, Chennai | DeitY, New Delhi | 2015 | 2020 | On going |
| Technology Incubation & Development of Entrepreneurs (TIDE) – Director/ CEDI | DeitY, New Delhi | 2012 | Till date | On going |
| Full Duplex and Cognitive Radio Architectures for Spectrally Efficient Communications (FD-CR-ASEC) | UKIERI - Department of S&T, New Delhi | | | Submitted on October 2016 |
| Bridging the Rural divIDe through enerGy neutral digital sErvices (BRIDGE) | EPSRC, UK | | | Submitted on November 2016 |

**14. (a) Patents:**

| SI.No. | Patents filed with detail | Patent issued | Patent Number |
|---|---|---|---|
| 1. | Improved wave pipelined array multiplier | May 15, 2008 | Indian Patent No. 220117 |
| **2.** | Design of Global Asynchronous Controller | March 01, 2013 | Patent filed in Indian patent office *** |

*** - Application Number: 596/CHE/2013, 12 February 2013, CBR No. 2025 published online on 01 March 2013 in official_journal_01032013_part_i.

15. Number of PhDs guided:

| Name of the PhD Scholar | Title of PhD Thesis | Role(Supervisor/ Co-Supervisor) | Year of Award |
|---|---|---|---|
| T.N.Prabakar | Design And Analysis of Schemes for the Implementation of Asynchronous Pipelined Circuits on FPGA | Co-Supervisor | 2011 |
| M.Santhi | Design and Analysis of High Performance MB-OFDM UWB Wireless System using Asynchronous Techniques | Supervisor | 2013 |
| C.Vennila | Design of reconfgurable architectures for base band processing in wireless communication system | Supervisor | 2013 |
| K.Swaminathan | Design of an efficient reliable interconnect fabric for network on chip | Supervisor | 2015 |
| V. Nithish Kumar | Design of Reconfigurable Spectrum sensing architecture for Cognitive radio and filter realization at gate level | Supervisor | 2016 |

**In addition:**

1. Number of Ph.Ds. ongoing as main guide: **09**
2. Number of M.S.(By Research) guided as main guide and degree awarded: **06**
3. Number of M.S.(By Research) ongoing as main guide: **03**

16. Participation in Workshops/ Symposia/ Conferences/ Colloquia /Seminars/ Schools etc. (mentioning the role)

| Date (s) | Title of Activity | Level of Event (International / National/ Local) | Role (Participant/ Speaker/ Chairperson, Paper presenter, Any other) | Event Organized by | Venue |
|---|---|---|---|---|---|
| 23rd to 25th Nov. 2010 | Cognitive Radio: The Next Frontier in Wireless Communications | National | Participant | IIT, Karagpur | ECE Dept. |
| 24th & 25th , Nov., 2008 | International SOC Design Conference (ISOCC) | International | Paper Presenter | Bexco, Busan, South Korea | Conference Hall |
| Every Year from 2008 to 2013 | ZOPP workshop | National | As Co-coordinator | IITs and IISc | ECE Dept. |

**In addition –**

1. **Lectures delivered in almost all the Engineering colleges of Tamil Nadu.**
2. **TPC member for Workshop, Symposium conducted by Engineering Colleges in Tamil Nadu & Hyderabad.**

17. Workshops/ Symposia/ Conferences/ Colloquia/Seminars Organized (as Chairman/ Organizing Secretary/ Convenor / Co-Convenor)

| Title of Activity | Level of Event (International/ National/ Local) | Date (s) | Role | Venue |
|---|---|---|---|---|
| A one day workshop on "Potential of UWB Wireless Technology | Local | 19th July 2008 | Convenor | NIT-Trichy |
| A two day workshop on "Design of High Performance Systems Using FPGAs" | National | 23rd and 24th Jan 2009 | Convenor | NIT-Trichy |
| A two day workshop on "An Overview of VLSI CAD TOOLS for Designing with Programmable Logic" | National | 17th and 18th Aug 2007 | Convenor | NIT-Trichy |

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|---|---|---|---|---|
| A week intensive course on "VLSI Realization of Digital Systems" | Local | | Convenor | Saranathan college of Engineering, Trichy |
| Reconfigurable Technology and its Applications | National | October, 2011 | Convenor | NIT-Trichy |
| A one day colloquium on Corrosion Control and Surface Engineering with a focus: R&D and industrial scenario, organized by CECASE, NIT, Trichy | National | 10 -12, Dec., 2012 | Convenor | NIT-Trichy |
| A 2 week programme on Entrepreneurship - Concept & Present Scenario with a fund of Rs. 1.75 lakhs sponsored by DST, New Delhi | National | June, 2013 | Convenor | NIT-Trichy |
| UKIERI Sponsored two day Workshop on "Advances in Cognitive Radio and its Hardware Implementation" | National | 23rd & 24th Dec 2014 | Convenor | NIT-Trichy |
| TEQIP sponsored workshop on "Evolution of 5G and IoT through cognitive Radio Networks" | National | 6th and 7th May 2016 | Co-convenor | NIT-Trichy |
| GIAN course on Design Techniques for Low Power High Performance VLSI Systems | National | 23rd Jan. 2017 to 30th Jan. 2017 | Co- convenor | NIT-Trichy |

18. Invited Talks delivered:

**Lectures delivered in almost all the Engineering colleges and Deemed Universities of Tamil Nadu & Hyderabad.**

19. Membership of Learned Societies

| Type of Membership (Ordinary Member/ Honorary Member / Life Member ) | Organization | Membership No. with date |
|---|---|---|
| Life Member | ISTE | Year of Induction:1995 |
| Member | IEEE | Member No.:41289382, Year of Induction: 2000 |

20. Academic Foreign Visits

| Country | Duration of Visit | Programme |
|---|---|---|
| Heriot-Watt University and University Of Edinburgh, U.K. | 18st Oct. to 28th Oct., 2013 | To do Collaboration under UKIERI Project |
| Bexco, Busan, South Korea | 24th & 25th , Nov., 2008 | Presented paper in International SOC Design Conference (ISOCC) |

**20. (a) Collaboration with Foreign Universities:**

| Ph.D. Student Visited Abroad | Duration | University Visited | Area and Foreign Supervisor |
|---|---|---|---|
| C. Vennila Arasu | Mar 2010 – Aug 2011 | University of Saskatchewan, Saskatoon, SK, Canada. | "Dynamic Partial Reconfigurable FFT for OFDM based Communication Systems" under the Guidance of Prof. Seok-Bum Ko. |
| K.Swaminathan | Sep 2011 – Feb 2012 | University of Saskatchewan, Saskatoon, SK, Canada. | "Design and Verification of Generic High Speed Network Interface for Network on Chip" under the Guidance of Prof. Seok-Bum Ko. |
| Geethu S | Aug 2012-Nov 2012 | Heriot Watt University, Edinburgh, United Kingdom | "Spectrum Sensing Algorithms for Cognitive Radio Networks" under the Guidance of Dr. Mathini Sellathurai. |
| Nithish Kumar V | Mar 2013 - Jun 2013 | Heriot Watt University, Edinburgh, United Kingdom | "Implementation of Spectrum Sensing Algorithm for Cognitive Radio Networks" under the Guidance of Dr. Mathini Sellathurai. |
| Antony Xavier Glittas | Oct 2014 - Dec 2014 | Heriot Watt University, Edinburgh, United Kingdom | "Implementation of FFT Processor and PAPR" under the Guidance of Dr. Mathini Sellathurai. |

21. Publications
(A) Refereed Research Journals:

| Author(s) | Title of Paper | Journal | Volume (No.) | Page numbers | Year | Impact Factor of the Journal (Optional) |
|---|---|---|---|---|---|---|
| G.Lakshminarayanan, B. Venkataramani | Optimization techniques for FPGA based wave pipelined DSP blocks | IEEE trans. on VLSI systems | 13 (7) | 783-793 | 2005 | |
| Nithish Kumar Venkatachalam, Lakshminarayanan Gopalakrishnan, Mathini Sellathurai | Low complexity and area efficient reconfigurable multimode interleaver address generator for multistandard radios | IET Computers & Digital Techniques | 10 (2) | 56-68 | 2016 | |
| Antony Xavier Glittas, Mathini Sellathurai, G.Lakshminarayanan | A Normal I/O Order Radix-2 FFT Architecture to Process Twin Data Streams for MIMO | IEEE trans. on VLSI systems | 24(6) | 2402-2406 | 2016 | |
| Antony Xavier Glittas, Mathini Sellathurai, G.Lakshminarayanan | Two-parallel Pipelined FFT Processors for Real-valued Signals | IET Circuits, Devices & Systems | 10 (4) | 330-336 | 2016 | |
| G. Seetharaman, B. Venkataramani and G. Lakshminarayanan | Design and FPGA implementation of self-tuned wave-pipelined filters with Distributed Arithmetic Algorithm | Springer, Research journal on circuits, systems and signal processing | 27 (3) | 261-276 | 2008 | |
| G. Seetharaman, B. Venkataramani and G. Lakshminarayanan | VLSI implementation of Hybrid wave-pipelined 2D DWT using lifting Scheme | Hindawi Publishing Corporation, Journal on VLSI | 2008(4) | 8 pages Article ID 512746 | 2008 | |
| C.Vennila, G.Lakshminarayanan, Seok-Bum Ko | Dynamic Partial Reconfigurable FFT for OFDM based Communication Systems | Circuits Systems and Signal Processing, Springer Verilog | 31 (3) | 1049-1066 | 2012 | |

| | | | | | | |
|---|---|---|---|---|---|---|
| M. Santhi, Siddharth Sarangan, K. Murali G. Lakshminarayanan | Performance analysis of pseudo 4-phase dual-rail asynchronous protocol | International Journal of Electronics, Taylor & Francis, Taylor & Francis | 99 (8) | 1108-1113 | 2012 | |
| C.Vennila, Alokkumarpatel, G.Lakshminarayanan, Seok-Bum Ko | Dynamic Partial Reconfigurable Viterbi decoder for wireless standards | Computer and Electrical Engineering, CAEE, Elsevier | 39 (2) | 164-174 | 2013 | |
| K.Swaminathan, G. Lakshminarayanan, Seok-Bum Ko | Design and Verification of an Efficient WISHBONE-based Network Interface for Network on Chip | Elsevier Journal of Computers & Electrical Engineering | 40 (6) | 1838–1857 | 2014 | |
| M.Santhi, G.Lakshminarayanan, B.Venkataramani | Design and Implementation of Online Clock Skew Scheme based Asynchronous Wave-Pipelined Distributed Arithmetic Filters on FPGA | IETE Journal of Research | 58 (6) | 494-500 | 2012 | |
| G.Lakshminarayanan, B.Venkataramani, G.Seetharaman | Design and FPGA implementation of self tuned wave pipelined filters | IETE Journal of Research | 52 (4) | 281-286 | 2006 | |
| G. Seetharaman, B. Venkataramani, G. Lakshminarayanan | Design and FPGA implementation of wave pipelined lifting scheme for two level 2D-DWT | WSEAS Transactions on Circuits and Systems | 10 (4) | 1284-1291 | 2005 | |
| M.Santhi, G.Lakshminarayanan | FPGA Based Asynchronous Pipelined MB-OFDM UWB Transmitter Backend Modules | International Journal of Communication and Technology | 1 (1) | | 2010 | |

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|---|---|---|---|---|---|---|
| M.Santhi, ArunKumar S, G S Praveen Kalish, Siddharth Sarangan, G. Lakshminarayanan | A Novel Pseudo 4 Phase Dual Rail Asynchronous Protocol With Self Reset Logic & Multiple Reset | International Journal of Computer Applications | 1 (21) | 17-21 | 2010 | |
| T. N. Prabakar, G.Lakshminarayanan, K. K. Anilkumar | Design and implementation of an Asynchronous controller for FPGA based asynchronous systems | International Journal of Computer Applications | 1 (21) | 23-29 | 2010 | |
| T. N. Prabakar, G. Lakshminarayanan, K. K. Anilkumar | Design and Implementation of an Asynchronous Controller for FPGA Based Biosignal Processing | International Journal of Computer Applications | 4 (4) | 34-37 | 2010 | |
| M.Santhi, G.Seetharaman, Roshan Silwal, G.Lakshminarayanan | Design and Implementation of Asynchronous WP DA FIR Filter using Online Clock Skew Scheme | IJDATICS | | | 2011 | |
| Geethu.s, Lakshminarayanan.g, MathiniSellathurai | Wide band Spectrum Sensing using Window based Energy Detector for AWGN and Rayleigh channels | International Journal of Engineering Research & Technology (IJERT) | 2 (5) | 91-96 | 2013 | |
| K. Swaminathan, G. Lakshminarayanan, Seok-Bum Ko | High Speed Low Power Ping Pong Buffering Based Network Interface for Network on Chip | Journal of Low Power Electronics | 9 (3) | 322-331 | 2013 | |
| Nithish Kumar V, Pani Prithvi Raj, Lakshminarayanan G, Mathini Sellathurai | Low Power and Area Efficient Carry Select Adder | Journal of Low Power Electronics | 10 (4) | 593-601 | 2014 | |

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|---|---|---|---|---|---|---|
| V. Nithish Kumar, Koteswara Rao Nalluri, G. Lakshminarayanan, Mathini Sellathurai | An Improved Recongurable FIR Filter using Common Subexpression Elimination Algorithm for Cognitive Radio. | Journal of Low Power Electronics | 11 (2) | 181-189 | 2015 | |

(B) Conferences/Workshops/Symposia Proceedings

| Author(s) | Title of Abstract/ Paper | Title of the Proceedings | Page numbers | Conference Theme | Venue | Year |
|---|---|---|---|---|---|---|
| X Antony Xavier Glittas, Lakshminarayanan G | Pipelined FFT architectures for Real-time Signal Processing and Wireless Communication Applications | 18th International Symposium on VLSI Design and Test (VDAT 2014) | 1-2 | Secure and Trustworthy System-on-Chip | Coimbatore, India | 2014 |
| C. Vennila , Kumar Palaniappan CT, Kodati Vamsi Krishna, G.Lakshminarayanan, Seok-Bum Ko, | Dynamic partial reconfigurable FFT/IFFT pruning for OFDM based Cognitive radio | 2012 IEEE International Symposium on Circuits and Systems | 33-36 | Convergence of BiNET | Seoul, Korea | 2012 |

**International conference papers**

1. G. Lakshminarayanan, Boby Geroge, B. Venkataramani, A. Ramakalyan , (1998) “Neural Network controlled Shift Register Traffic Shaper for ATM Networks” ,pp 33 - 36 , vol.1, TENCON.

2. G. Lakshminarayanan, B. Venkataramani, M. Sasitharan, K.P. Senthil Kumar, (2000) “Design and Implementation of FPGA based wavepipelined multiplier accumulators", Proc. of the International Conf. on Circuits, Control, Communication and Devices, ICCCD’ 2000, VOL. I, No.59, pp.265-268.

3. G. Lakshminarayanan, B. Venkataramani, K.P. Senthil Kumar, M. Sasitharan, (2000) V.A. Kiran Kottapalli, "Design and implementation of FPGA based wave pipelined Fast Convolver", Proc. of the International Conf. TENCON 2000, Kuala Lumpur, Malaysia, VOL. III, No.212, pp. 212-217.

4. G. Lakshminarayanan, B. Venkataramani, J. Senthil Kumar, A.K. Md. Yousuf, G. Sriram, (2003) “Design and FPGA Implementation of Image Block Encoders with 2D-

DWT", Proc. of the International Conf. TENCON 2003, India, SessionZ04, pp.1015-1019 ,Advanced DSP-II.

5. G. Seetharaman, B. Venkataramani, and G. Lakshminarayanan, (2005) "Design and FPGA implementation of lifting scheme for 2D-DWT using wave pipelining, Proc. of the 5th Int. conf. on Signal processing, Computational Geometry & Artificial Vision, pp.53-60.

6. G. Lakshminarayanan and T.N. Prabakar, (2007) "On-Board Verification of FPGA Based Digital Systems Using NIOS Processor (A methodology without Hook-Ups and I/O Cards)", International Conference on Signal Processing, Communications and Networking, pp 596 – 598, ICSCN .

7. T.N.Prabhakar, G.Lakshminarayanan, K.K.Anilkumar, (2008) "FPGA Based Asynchronous Pipelined Multiplier with intelligent delay controller", IEEE SOC Design Conference, pp: I-304 - I-309.

8. M.Santhi, Sowjanya Tungala, Balakrishna.C, G.Lakshminarayanan, (2009) "Asynchronous Pipelined MB-OFDM UWB Transceiver on FPGA" presented in IEEE TENCON, Singapore.

9. T.Kumaran, M.Santhi, M.Srikanth, Narayana Srinivasan, M.Balaj,G.Lakshminarayanan, (2009) "Transient Current Sensing Based Completion Detection with Event Separation Logic for High Speed Asynchronous Pipelines", presented in IEEE TENCON.

10. M.Santhi, G.Lakshminarayanan, R.Sundaram, N.Balachandar, (2009) "Synchronous Pipelined Two-Stage Radix-4 200Mbps MB-OFDM UWB Viterbi Decoder on FPGA", IEEE ISOCC.

11. M.Santhi, Surya vamshi vardhan, Dr.G.Lakshminarayanan (2009) FPGA based Asynchronous Pipelined Viterbi Decoder using Two Phase Bundled-Data Protocol -, , IEEE, ISOCC.

12. M.Santhi, G.Seetharaman, Roshan Silwal, G.Lakshminarayanan, (2010) "A Novel Online Clock Skew Control Circuit for Asynchronous Wave pipelining on FPGA", selected for presentation in IEEE DATICS Futuretech'10, Busan, Korea.

13. Sanjay G. Talekar, S. Ramasamy, G. Lakshminarayanan and B. Venkataramani (2009) "500MS/s 4-b time interleaved SAR ADC using novel DAC architecture" 1st Asia Symposium on Quality Electronic Design, pp 202-205.

14. Sanjay G. Talekar, S. Ramasamy, G. Lakshminarayanan and B. Venkataramani (2009) "Low power 700MSPS 4-bit 2bit/step time interleaved SAR ADC in 0.18μm CMOS", pp: 1 – 5, EDAS IEEE-RSM 2009 conference, Malaysia.

15. Sanjay G. Talekar, S. Ramasamy, G. Lakshminarayanan and B. Venkataramani (2009) "A Low power 700MSPS 4-bit time interleaved SAR ADC in 0.18µm CMOS", pp: 1 - 5 , Singapore, TENCON 2009.

16. T.N. Prabakar, Dr. G. Lakshminarayanan and Dr. K.K. Anilkumar, (2007) "SOPC based Asynchronous Pipelined DCT with self testing capability", accepted for presentation in the IEEE International Conference on Microelectronics - IEEE ICM-07, Cairo, Egypt.

17. C.Vennila, G.Lakshminarayanan, ArpitRaj, Anandkrishnan, Santhosh, Mithun Reddy, Vijaykumar, (2010) "Design of Self-Reconfigurable Task-Scheduler to Implement Multi-Rate MB-OFDM UWB Wireless Systems", 2010 Intl Conf on Electronic Devices, Systems and Applications (ICEDSA), pp-37-42, Kualalampur, Malaysia.

18. C.Vennila Arasu, Alok Kumar Patel, Jaimil Upadhyay, G. Lakshminarayanan, and S. Ko, (2011) "High Speed Reconfigurable Viterbi Decoder for Wireless Standards," 15th International Workshop on Multimedia Signal Processing & Transmission, pp. 114-119, Jeonju,Korea.

19. C.VennilaArasu, Satyashil Nagrale, G.Lakshminarayanan,(2011) "FPGA implementation of adaptive mode PAPR reduction for cognitive radio applications", International Conference on Communication Systems and Network Technologies, pp. 444-448, Katra, Jammu.

20. M.Santhi, G.Lakshminarayanan, Sowjanya Tungala, Balakrishna.C, (2009) "FPGA Based Asynchronous Pipelined OFDM for MB-OFDM UWB Application", IEEE International Conference on Control, Automation, Communication and Energy Conservation (INCACEC), Tamilnadu, India, pp. 1-6.

21. M.Santhi, G.Lakshminarayanan, Sowjanya Tungala, Balakrishna.C, (2009) "Design of Low Power Asynchronous Pipelined Systems with Input Change Detection Circuit", IEEE International Conference on Control, Automation, Communication and Energy Conservation (INCACEC), pp. 1-6.

22. M.Santhi, M.Shravan kumar, T.N.Prabhakar, Dr.G.Lakshminarayanan, (2008) "Design and Implementation of pipelined MB-OFDM UWB transmitter back end modules on FPGA" -, IEEE ICCCN, Karur, Tamilnadu.

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